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Design and implementation of control system for superconducting RSFQ circuit①

ZHANG Kuozhong(张阔中)[*,**], HUANG Junying[*], ZHANG Hui[***], TANG Guangming[*], ZHANG Zhimin②[*], YE Xiaochun[*]

([*]State Key Laboratory of Processors, Institute of Computing Technology, Chinese Academy of Sciences, Beijing 100190, P. R. China)

([**]University of Chinese Academy of Sciences, Beijing 101408, P. R. China)

([***]Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences, Shanghai 200050, P. R. China)

Abstract

The superconducting rapid single flux quantum (RSFQ) integrated circuit is a promising solution for overcoming speed and power bottlenecks in high-performance computing systems in the post-Moore era. This paper presents an architecture designed to improve the speed and power limitations of high-performance computing systems using superconducting technology. Since superconducting microprocessors, which operate at cryogenic temperatures, require support from semiconductor circuits, the proposed design utilizes the von Neumann architecture with a superconducting RSFQ microprocessor, cryogenic semiconductor memory, a room temperature field programmable gate array (FPGA) controller, and a host computer for input/output. Additionally, the paper introduces two key circuit designs: a start/stop controllable superconducting clock generator and an asynchronous communication interface between the RSFQ and semiconductor chips used to implement the control system. Experimental results demonstrate that the proposed design is feasible and effective, providing valuable insights for future superconducting computer systems.

Key words: single flux quantum, superconducting rapid single flux quantum (RSFQ) circuit, superconducting control system, clock generator, asynchronous communication interface circuit

0 Introduction

Currently, digital integrated circuits based on complementary metal oxide semiconductor (CMOS) technology are close to the physical limit, making it difficult to match the rapid progress predicted by Moore's law[1]. As a result, researchers are exploring new directions for integrated circuit development. In 1911s, Dutch physicist Onnes discovered that mercury has a resistance close to zero when the temperature drops to 4.2 K, a state known as superconductivity. In 1962s, Josephson[2] proposed the Josephson effect of superconducting electrons, which was soon confirmed experimentally. Based on this discovery, Refs [3-4] proposed the rapid single flux quantum (RSFQ) circuit in the mid-1980s, which uses Josephson junction (JJ) as switches. This superconducting RSFQ circuit is a new technology that can increase working speed by 2-3 orders of magnitude and reduce power consumption by 3 orders of magnitude compared with traditional semiconductor circuits[5]. It is expected to solve the speed and power bottlenecks faced by high-performance computing in the post-Moore era. It has been confirmed that the RSFQ TFF (T flip-flop) cell can operate at a maximum frequency of 770 GHz[6].

Despite numerous proposed circuit designs based on RSFQ, such as arithmetic logic unit[7-11], cryptographic algorithm accelerators[12-13], neural network accelerators[14], and superconducting quantum controllers[15], most research has focused on the logic design of single chips, with few reports on complete superconducting computer systems. While some physical chips have been verified, there is currently no comprehensive system design in place. This paper presents a first control system design for superconducting circuits, enabling the realization of complete superconducting computing systems.

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② To whom correspondence should be addressed. Email: zzm@ict.ac.cn.

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Since superconducting RSFQ circuits operate in a low-temperature environment of 4.2 K (−268.95 ℃), it is currently impossible to immerse the entire system in liquid helium. Therefore, building a practical superconducting computing system still requires the assistance of semiconductor circuits. Following the von Neumann architecture, the proposed control system comprises four components. The superconducting RSFQ circuit primarily focuses on the calculation function and can serve as the central processing unit (CPU) to some extent. The remaining control system components, namely the cryogenic semiconductor memory chip, room temperature field programmable gate array (FPGA), and host computer, still require existing CMOS technology to be implemented.

Due to process technology limitations, current superconducting memory integration is unable to store a large amount of data. The proposed superconducting RSFQ circuit control system utilizes a cryogenic CMOS memory chip for memory storage, which can work in the low-temperature environment. The superconducting RSFQ circuit internally uses single magnetic flux quantum pulses for data processing and storage, while CMOS circuits use voltage level signals for operation. To enable communication between the superconducting RSFQ CPU and the CMOS cryogenic memory, an interface circuit that can match the high-speed pulse signal of the superconducting circuit and the low-speed level signal of the CMOS circuit for asynchronous communication is required.

Most existing superconducting circuits use return-to-zero (RZ) conversion cells to convert level signals to pulse signals by triggering the external input level signal's rising edge. This level/pulse conversion cell is simple and suitable for clock and control signal input, and is widely used[5]. However, RZ conversion cells become uncontrollable and unpredictable when processing data input signals because the external signal input's rising edge can arrive at the wrong time, leading to timing errors in the superconducting RSFQ circuit. To address this issue, researchers proposed a non-return-to-zero (NRZ) level/pulse conversion cell[16]. The NRZ conversion cell utilizes the clock signal inside the RSFQ circuit to synchronize the conversion action and has been applied in some superconducting circuit designs[17]. The asynchronous communication interface circuit proposed in this paper adopts NRZ conversion cells to sample the data input signal.

One characteristic feature of superconducting RSFQ circuits is that most of their logic gates require clock signals for operation. However, if the clock signal is supplied by an external CMOS circuit, it must be converted from a level signal to a pulse signal using a DC/SFQ conversion cell. This conversion limits the clock frequency to the highest operating frequency of the conversion cell and makes the externally provided clock signal susceptible to electromagnetic interference at high frequencies. To fully utilize the benefits of the high operational frequency of superconducting circuits, developing an on-chip high-speed clock generator is essential. Furthermore, the clock generator must be controllable by the FPGA controller.

In summary, this paper proposes the following key contributions.

This paper proposes a control system for superconducting RSFQ circuits that comprises a superconducting RSFQ CPU, CMOS cryogenic memory, FPGA controller, and host computer.

Additionally, a start/stop controllable clock generator based on superconducting RSFQ logic has been designed, providing a stable on-chip clock source for superconducting RSFQ circuits.

Moreover, an interface circuit for asynchronous communication between the superconducting RSFQ circuit and the CMOS circuit has been proposed, which enables asynchronous data reading and writing between the RSFQ CPU and cryogenic memory.

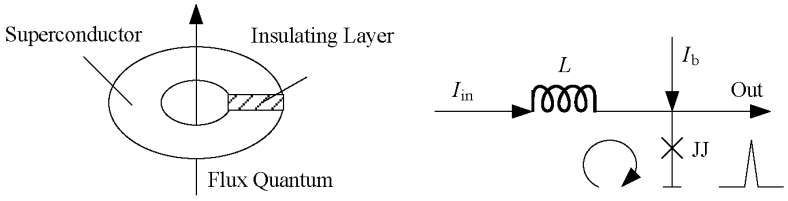
Finally, the proposed superconducting RSFQ circuit control system has been implemented with a test chip, achieving correct data reading and writing between the superconducting RSFQ CPU test chip operating at 1 GHz frequency and the CMOS cryogenic memory operating at 5 MHz frequency. These results confirm the feasibility and effectiveness of the proposed control system and key circuit design. Overall, this paper presents significant contributions towards the development of complete superconducting computing systems.

1 Background and motivation

1.1 Josephson junction

The superconducting RSFQ circuit consists of Josephson junctions (JJs), as shown in Fig. 1(a). The JJ comprises a superconductor (such as niobium metal) and an oxide insulation layer (such as AlOx) with a thickness of about 2 – 3 nm, and the ring structure of the superconductor and the insulation layer form the Josephson junction. Fig. 1(b) illustrates the equivalent circuit where a bias current (I_b) is applied to the junction, which is typically 70% of the threshold current. When an input current pulse (I_{in}) occurs, the sum of I_b and I_{in} exceeds the JJ threshold current, generating a tunneling current and forming a stable single

flux quantum (SFQ) in the ring. The superconducting RSFQ logic represents binary logic '1' and '0' based on the presence or absence of SFQ in the Josephson junction. Information is stored and transmitted in the form of SFQ. Overall, the JJ plays a critical role in the operation of superconducting RSFQ circuits and enables the high-speed, low-power operation that is characteristic of these circuits.



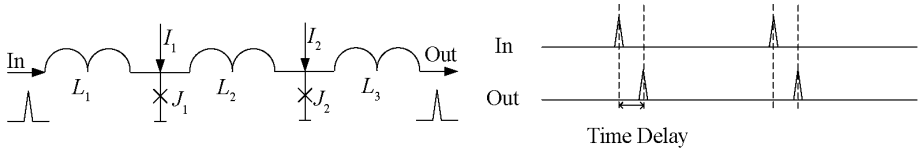
(a) Physical structure of a Josephson junction (b) Equivalent circuit

Fig. 1 Schematic diagram of JJ

The basic cell of a superconducting RSFQ circuit mainly includes a pulse transmission line, level/pulse signal conversion cell, and logic gates [16].

1.2 Pulse transmission line

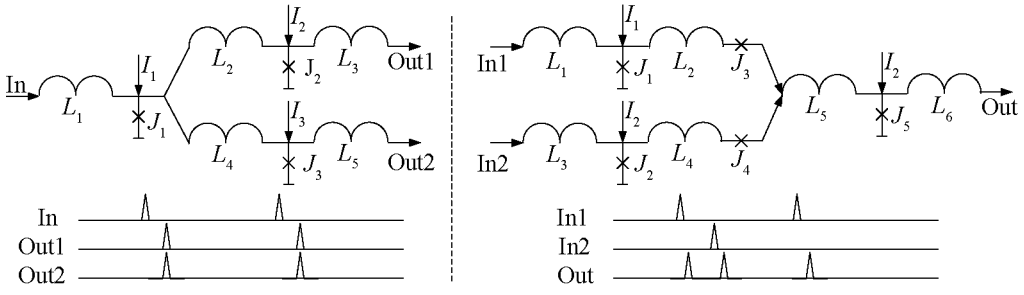
The SFQ pulses can be transmitted through the Josephson transmission line (JTL) inside the RSFQ circuit, as shown schematically in Fig. 2(a). When an SFQ pulse enters the input port of the JTL, it will activate subsequent adjacent Josephson junctions in turn to transmit the pulse signal to the output port. During the SFQ pulse transmission process, there is a certain time delay from the input port to the output port, which is the transmission time delay of JTL. The JTL plays a crucial role in facilitating the transmission of SFQ pulses between different parts of the RSFQ circuit and is an essential component in the operation of superconducting RSFQ circuits.



(a) Schematic of JTL (b) Waveform of JTL

Fig. 2 Schematic diagram of a Josephson transmission line (JTL)

Due to the quantum characteristics of the SFQ pulse signal, the driving capacity of each cell in the RSFQ circuit is limited, and the fan-out value can only be 1. Therefore, when multiple fan-out signals are required in the circuit, a specialized cell called a splitter (SPL) needs to be inserted, as shown in Fig. 3(a). The SPL cell takes an input pulse and splits it into two output pulses, enabling multiple connections to be made to other parts of the circuit. Similarly, the confluence buffer (CB) is used to combine two input pulse signals into one output pulse, as shown in Fig. 3(b). Overall, the SPL and CB cells play a crucial role in enabling multiple connections to be made in the superconducting RSFQ circuit while maintaining the quantum characteristics of the SFQ pulse signal.

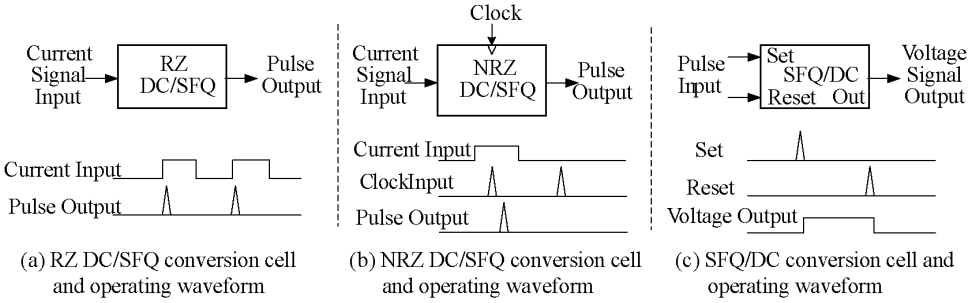


(a) Schematic and waveforms of SPL (b) Schematic and waveforms of CB

Fig. 3 Schematic diagram of SPL and CB

1.3 Level/pulse signal conversion cell

The DC/SFQ conversion cell, which converts a level signal into an SFQ pulse signal, has two forms. One is the RZ DC/ SFQ cell, as shown in Fig. 4(a). The input to the RZ DC/ SFQ cell is a current signal. When the current value of the input conversion cell is greater than the threshold of the conversion cell, an SFQ pulse will be generated inside it, and this is reflected as the rising edge of the input level being converted to an SFQ pulse output.



(a) RZ DC/SFQ conversion cell and operating waveform

(b) NRZ DC/SFQ conversion cell and operating waveform

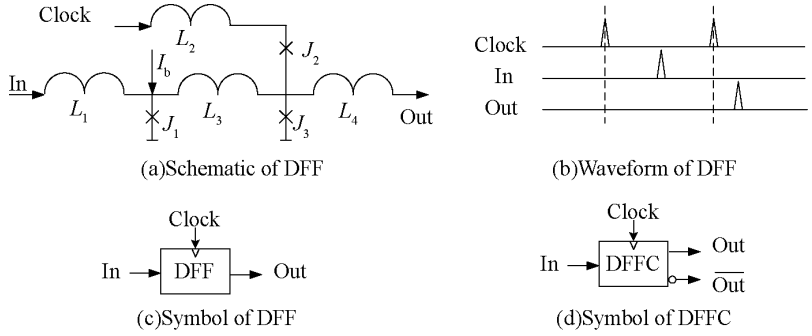
(c) SFQ/DC conversion cell and operating waveform

Fig. 4 DC-SFQ conversion cell

The other conversion cell is the NRZ-DC/SFQ, which is a three-port cell with a clock input, as shown in Fig. 4(b). When the clock signal arrives, if the input port has a current signal input, an SFQ pulse will be generated at the output port [18]. The SFQ/DC conversion cell, which converts the SFQ pulse signal into a voltage level signal, is shown in Fig. 4(c). When the (Set) port has an SFQ pulse signal input, the output port (Out) produces a stable high-level output. Conversely, when the (Reset) port has an SFQ pulse signal input, the output port becomes a zero voltage. In the current superconducting RSFQ process library, the typical output voltage amplitude is 0.2 mV. The DC/SFQ and SFQ/DC conversion cells are essential components in the superconducting RSFQ circuit, enabling the conversion of signals between level and SFQ pulse formats.

1.4 Basic logic gates

The superconducting D flip-flop (DFF) is a crucial logic cell used to perform digital circuit operations. The schematic circuit is shown in Fig. 5(a), and its operating waveform is shown in Fig. 5(b). In the circuit logic design of this article, a DFF with complementary outputs (DFFC) is used, and the symbols of the two are shown in Fig. 5(c) and Fig. 5(d), respectively.



(a)Schematic of DFF

(b)Waveform of DFF

(c)Symbol of DFF

(d)Symbol of DFFC

Fig. 5 Schematic diagram of DFF cell

Common logic gates used in superconducting RSFQ circuits include XOR, NOT, and AND gates, all of which are driven by clock signals. After the clock signal is input, these gates can perform XOR, negation, and AND operations with the data entered in the previous clock cycle. These gates are fundamental building blocks of digital circuits and enable the implementation of various complex functions on superconducting RSFQ circuits.

1.5 Comparison of RSFQ logic and CMOS logic

As a new digital circuit implementation method based on single flux quantum, superconducting RSFQ circuits are very different from traditional CMOS circuits. Table 1 compares the differences between superconducting RSFQ circuits and CMOS circuits. Compared with traditional semiconductor circuits, the working speed of RSFQ circuits can be increased by 2 – 3

orders of magnitude, and the power consumption can be reduced by 3 orders of magnitude [6]. These advantages are due to the unique characteristics of superconducting RSFQ circuits. However, because of the differences between RSFQ and CMOS circuits, the design of control systems for RSFQ circuits should consider asynchronous communication problems that may arise when interfacing with CMOS circuits. Despite these challenges, the advantages offered by superconducting RSFQ circuits make them an exciting area of research for future digital circuit implementation.

Table 1 RSFQ circuit vs. CMOS circuit

	RSFQ circuit	CMOS circuit
Component devices	JJ	Field effect transistors
Logical representation	SFQ pulse	Voltage level
Fan-out capability	1	>1
Interconnect wires	JTL	Metal wire
Power supply mode	Bias current	Voltage source
Signal amplitude	0.2 mV	1.2 V
Operating frequency	10 – 100 GHz	1 GHz
Power consumption	mW level	W level

1.6 Research challenges and goal

Although superconducting computers offer promising advantages such as high-speed and low-power consumption in high-performance computing scenarios, it has been challenging to validate these potentials using practical high-performance applications. This is due to the absence of a complete superconducting computer system architecture that accurately analyzes the target application's performance on the superconducting computer system. To develop such a superconducting computer system, particularly in the control system, architects need to address the following challenges.

(1) Absence of architectural design for superconducting control systems. The lack of an architectural design for superconducting control systems presents a significant challenge for architects seeking to demonstrate the advantages of RSFQ technology in terms of performance and power efficiency. While researchers have studied RSFQ microprocessors and superconducting accelerators, a system-level design from an architectural perspective is still needed, as well as a demonstration of the system's application.

(2) Lack of communication scheme between superconducting and semiconductor logic. To design an effective quantum computing system based on superconducting technology, the industry and research community have been exploring various target temperatures (e.g., 300 K, 4 K) and device technologies (e.g., RSFQ, ERSFQ, CMOS).

(3) However, a major challenge remains the lack of a communication scheme between the superconductor and semiconductor logic. Specifically, there has been limited investigation into the design of a communication interface between RSFQ and CMOS circuits, which is critical to enable asynchronous communication. To address this gap, comprehensive research is needed to provide clear design guidelines for such an interface.

In this paper, the challenges are addressed by fully implementing a robust control system architecture (Section 2), proposing an asynchronous communication interface circuit (Section 3), and presenting experimental results of the developed superconducting control system (Section 4).

2 Superconducting RSFQ circuit control system design

This paper proposes a control system design for superconducting circuits, which is the first of its kind. The system architecture, as illustrated in Fig. 6, consists of four components: a superconducting RSFQ CPU, CMOS cryogenic memory, FPGA controller, and host computer.

2.1 Superconducting RSFQ CPU

The control system proposed in this paper is designed to support a superconducting RSFQ CPU that reads instructions and data from the cryogenic memory and writes the calculation results back to the memory. The architecture can accommodate different instruction sets and microstructures for the superconducting RSFQ CPU.

2.2 CMOS cryogenic memory

As of now, manufacturing large-scale RSFQ memory remains a challenge. Therefore, this paper's proposed superconducting RSFQ circuit control system utilizes cryogenic CMOS circuits as memory. To reduce the number of cross-temperature connection lines be-

tween room temperature and the cryogenic temperature of the superconducting circuits, the memory is designed with dual-port read/write functionality. One port can be read and written by the superconducting RSFQ CPU to provide instructions and operation data, while the other port can be read and written by the FPGA controller.

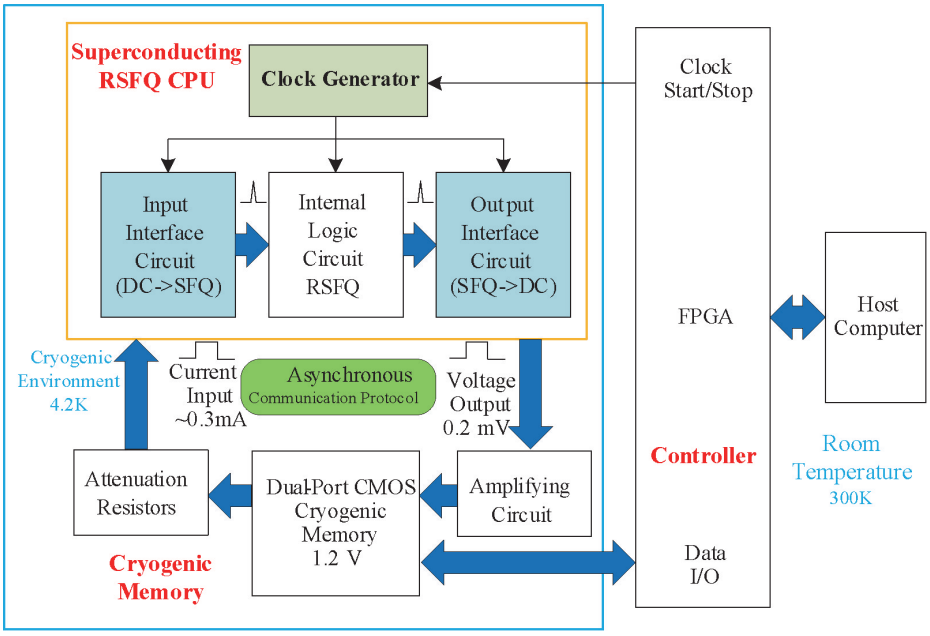


Fig. 6 Architecture of superconducting RSFQ circuit control system

2.3 FPGA controller

The superconducting RSFQ circuit control system designed in this paper utilizes a field-programmable gate array (FPGA) as the controller due to its high flexibility and reconfigurability. Acting as a bridge between the cryogenic and room temperature systems, the controller is responsible for controlling the working state of the superconducting RSFQ CPU and memory in the cryogenic environment, as well as connecting all signal lines between the two systems.

2.4 Host computer

The host computer compiles the instructions and data that the superconducting RSFQ CPU needs to execute. It is also the human-computer interaction port of the entire superconducting circuit control system, allowing users to view the operation results.

2.5 Control system operation logic

The application algorithm is compiled into a binary file by the host computer and stored in the CMOS cryogenic memory through the FPGA controller. The superconducting RSFQ CPU reads the instruction data from the cryogenic memory and writes the calculation results back with a current signal of approximately 0.3 mA. Due to the low output level of the superconducting RSFQ CPU (around 0.2 mV), an amplification circuit is required to drive the cryogenic CMOS memory directly. This paper also presents two key circuit designs: the clock generator and RSFQ-CMOS asynchronous interface circuit, both of which are crucial to ensuring the proper functioning of the system. The typical operation process of the superconducting RSFQ circuit control system proposed in this section is as follows.

(1) Write an application in the host computer, and obtain a binary source file that meets the requirements of the superconducting operator instruction set through cross-compilation.

(2) The host computer writes the compiled binary file to the cryogenic memory through the FPGA controller.

(3) The FPGA controller starts the superconducting RSFQ clock generator, and the superconducting RSFQ CPU enters the high-speed working, and the cryogenic memory provides the instructions and operation data.

(4) The superconducting RSFQ CPU completes the operation, and the FPGA controller sends a stop signal to the clock generator, then to read the cryogenic memory.

(5) Check the calculation results retrieved by the FPGA controller through the host computer. For single-

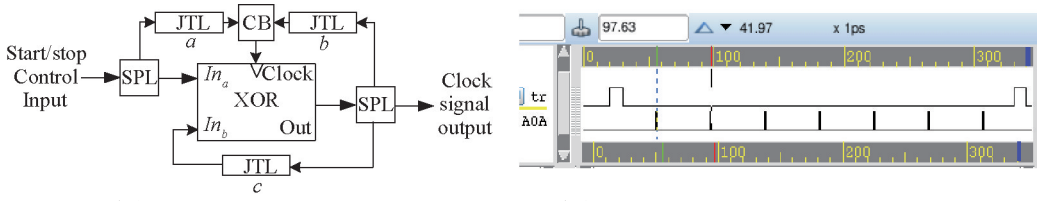
core superconducting RSFQ CPU, the running process can realize a single-pass batch system, which can better play the advantages of high operating frequency of superconducting RSFQ CPU.

3 Key circuit design

3.1 Clock generator

Superconducting RSFQ circuits use single flux quantum pulses for data transfer and calculation, with most logic gates requiring clock signals to operate. The frequency of the clock signal provided externally is limited by the operating frequency of the DC/SFQ conversion cell. High-frequency clock signals are also prone to electromagnetic interference. Thus, a stable on-chip clock source is critical in the design of superconducting RSFQ circuits.

The on-chip clock generator for classic superconducting RSFQ circuits is typically composed of a simple toroidal JTL structure that cycles the pulse output after a magnetic flux pulse is received. This structure allows for high clock frequencies. However, the clock generator cannot be stopped by logic control alone and relies upon cutting off the current bias of the relevant cells to stop the pulse signal. This control method leads to superconducting circuit instability, making it unsuitable for large-scale superconducting circuit systems. This section proposes a logically controlled on-chip RSFQ clock generator based on an XOR gate. The logical structure of this clock generator is shown in Fig. 7(a), where a, b, and c represent the delay time of JTL.



(a) Logic diagram of RSFQ clock generator (b) Waveform of RSFQ clock generator

Fig. 7 RSFQ clock generator schematic

Startup of the clock generator: when the first start/stop control pulse signal arrives at the input port, it is input to the In_a port and the Clock port through a splitter (SPL). The start/stop control pulse signal first reaches the In_a data input port because the delay time of JTL before CB is a ($a > 0$). It then reaches the *Clock* port. At this point, the data input state of the XOR gate is $In_a = 1$, $In_b = 0$, and after calculation, it outputs 1, producing the first pulse signal output at the *Out* port.

After this, the XOR gate enters the cyclic state, continuously generating pulse signals at the *Out* port. The clock signal output has a stable frequency with a period of $T = b + t_{\text{delay}}$, where t_{delay} is the sum of the propagation delay of the SPL and CB and the XOR gate operation delay. The period T of the clock generator can be adjusted by controlling the JTL time delay (b) in the circuit design.

Stop of the clock generator: during the working process of the clock generator, if the start/stop port receives another pulse signal, which serves as the stop signal, it will reach the In_a port through the SPL and provide an additional clock pulse. At this time, there is a high probability that the In_b input of the XOR gate has a pulse input, resulting in an input state of $In_a = 1$, $In_b = 1$. After the calculation of the XOR gate, the output will be 0, thus stopping any further pulse generation.

The clock generator's simulation waveform is shown in Fig. 7(b), demonstrating that the clock generator can output clock pulses up to 23.8 GHz.

3.2 Asynchronous communication protocol

The interface circuit design for asynchronous communication between the superconducting RSFQ CPU and the CMOS cryogenic memory must meet the following requirements.

(1) The interface definition should be as simple as possible, and the number of interface connections minimized to reduce the chip area.

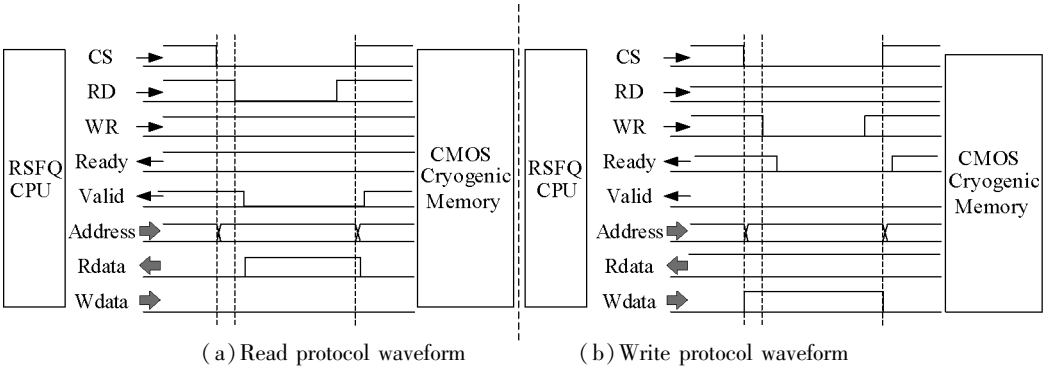
(2) Since the internal clock frequency of the superconducting RSFQ CPU is fast while the operating frequency of the CMOS cryogenic memory circuit is slow, the rate matching problem of the two circuits should be considered.

(3) As the core circuit, the superconducting RSFQ CPU will actively initiate communication requests. The cryogenic memory must timely respond to read/write requests and feedback whether it is in a working state.

To meet the above requirements, this article proposes a communication protocol comprising three parts: control lines, address bus, and data bus. The control lines include the chip select signal (CS), read request (RD), and write request (WR). Since the superconducting RSFQ CPU does not initiate read/write requests simultaneously, the read/write address shares a set of the address bus. The data bus comprises the write-out data bus (Wdata) of the superconducting RSFQ CPU and the read data bus (Rdata) sent to the CPU by cryogenic memory.

Due to the low operating frequency of cryogenic memory, it is necessary to provide feedback on its own status and data validity information to the CPU for asynchronous handshaking. The (Valid) control line indicates that the memory has output valid data after receiving the read request. The CPU determines whether it can read data based on whether the (Valid) line is set. To avoid interference pulses, the control signal is active low, following the anti-interference strategy of the CMOS circuit.

The status signal (Ready) indicates the current state of the cryogenic memory and whether it can receive read/write request signals. The CPU reads and writes when the (Ready) signal is asserted; otherwise, it waits until the (Ready) signal is restored. Fig. 8 shows the operating waveform of this protocol.



(a) Read protocol waveform (b) Write protocol waveform

Fig. 8 Working waveforms of the asynchronous communication protocol

3.3 Asynchronous communication interface circuit design

This section proposes a superconducting RSFQ interface circuit designed to convert the RSFQ CPU's pulse signal and the cryogenic memory voltage level signal. The interface comprises the input interface circuit and output interface circuit of the superconducting RSFQ CPU. The circuit logic is shown in Fig. 9.

The input interface circuit is designed to convert the voltage level signal sent by the cryogenic memory into a pulse signal using NRZ-DC/SFQ conversion cells. According to the asynchronous communication protocol, when the CMOS circuit outputs valid data (Rdata), the Valid signal is set to a low level. To accommodate this, a non-logic gate NOT is added to reverse the pulse sampled by the Valid signal. The output pulse of the NOT cell serves as the clock signal of the data sampling cell NRZ-DC/SFQ. This saves the clock tree wires of the data sampling cell and reduces the unnecessary reading of the input data (Rdata).

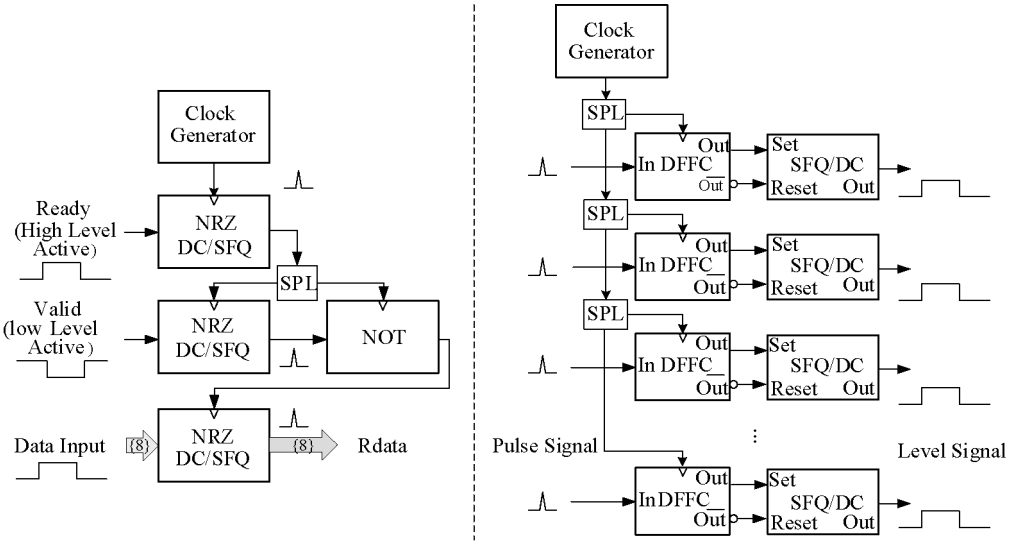
The Ready status control signal is also considered in the input interface circuit design. The NRZ sampling output pulse of the Ready signal is the clock signal of the subsequent circuit. The subsequent circuit works only when *Ready* = 1. If *Ready* = 0, the subsequent data input circuit stops working due to no clock signal.

For the superconducting RSFQ output interface circuits, the process is to convert the SFQ pulses into voltage-level signals recognizable by the CMOS cryogenic memory for processing. The output interface circuit is shown in Fig. 9(b). A DFFC with complementary output ports is used, and a DFFC array is formed at the output, driven by a synchronous clock signal. The complementary output DFFC characteristics match the input characteristics of the SFQ/DC conversion cell: the positive output port of the DFFC is connected to the set port (Set) of the SFQ/DC conversion cell, and the reverse output port is connected to the reset port (Reset). If the superconducting circuit produces a pulse output in a clock cycle, the output of the SFQ/DC conversion cell produces a high voltage level. With this output interface circuit, the superconducting RSFQ circuit's output signal can be converted from a pulse to a voltage level signal.

3.4 Put all together

The architecture of the asynchronous communication circuit in the superconducting RSFQ circuit control

system can be designed based on the superconducting RSFQ key circuit design described above. The superconducting RSFQ CPU communicates asynchronously with the CMOS cryogenic memory via the interface circuit. The on-chip RSFQ clock generator synchronously coordinates the internal working sequence of the CPU and provides a clock pulse for the entire RSFQ circuit, including the input/output interface circuit. The input interface circuit reads the data required by the CPU from the cryogenic memory, converts the level signal into a pulse signal, and provides it to the subsequent internal logic circuit of the CPU for processing. Since the amplitude of the level signal output by the CMOS cryogenic memory is 1.2 V, a set of attenuation resistors is required to reduce the signal current to 0.3 mA. The output interface circuit converts the CPU's pulse signal into a 0.2 mV level signal. Therefore, an amplification circuit is required to increase the signal voltage to 1.2 V, which can be recognized by the CMOS cryogenic memory. The relevant design work of the amplification circuit can be found in Ref. [19]. The superconducting RSFQ CPU operates in the high-frequency clock domain, and the cryogenic memory operates in the low-frequency clock domain. They communicate asynchronously through the interface circuits proposed in this section. The circuit architecture is shown in Fig. 10.



(a) Input interface (b) Output interface

Fig. 9 Logic diagram of superconducting RSFQ circuit

4 Experiments

As no previous literature has reported on the design of a superconducting computer system, this paper presents a first complete superconducting RSFQ circuit control system. Thus, this work has demonstrated the effectiveness of the proposed RSFQ circuit control system through practical testing.

4.1 Experiment setup

The RSFQ CPU test chip is in complete accordance with the logic design proposed in this paper to build its interface circuit. It is produced by the Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences using SIMIT Nb03 process library [20]. The cell library's main technical indexes are: Jc = 6 kA/cm^2, the Josephson junction density on the chip is 10^4 JJs/cm^2 with 4 layers of metal. This cell library is designed to operate at a maximum frequency of 25 GHz and has been included in the 2020 IRDS [21].

The overall architecture of the proposed superconducting RSFQ circuit control system is shown in Fig. 11. The cryogenic system is located in a liquid helium Dewar tank operating at 4.2 K. Multiple chips are integrated on a cryogenic PCB board. Due to the limitations of the chip manufacturing process, amplifying the 0.2 mV level signal output by the RSFQ circuit to 1.2 V requires a two-stage amplification chip. The cryogenic memory chip has a capacity of 1 kB operating at 1 GHz. The cryogenic PCB test board is connected to the FPGA controller in the room temperature environment through the cross temperature zone adapter rod and high-frequency shield wires to transmit 1.2 V level signals. The room temperature system includes the FPGA controller and a host computer.

The superconducting RSFQ CPU test chip can re-

alize 8-bit data read/write function. Its input ports include control signal ports (Ready/Valid), an 8-bit read data bus (Rdata), clock generator start/stop control port, system reset port, and others. Among them, the Ready/Valid signal and Rdata are sampled by NRZ-DC/SFQ conversion cells, following the aforementioned design, while the other input ports use traditional RZ-DC/SFQ conversion cells. Output ports include CS/RD/WR, a 10-bit address bus (Address), an 8-bit write data bus (Wdata), and other status monitoring ports.

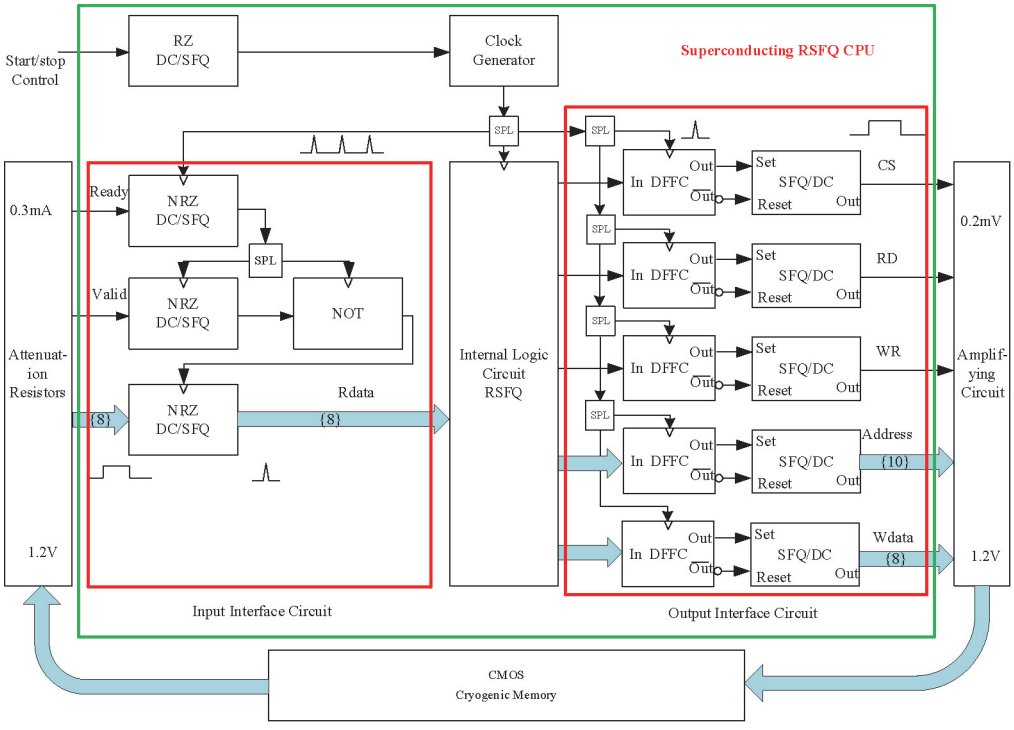


Fig. 10 Logic diagram of asynchronous communication circuit

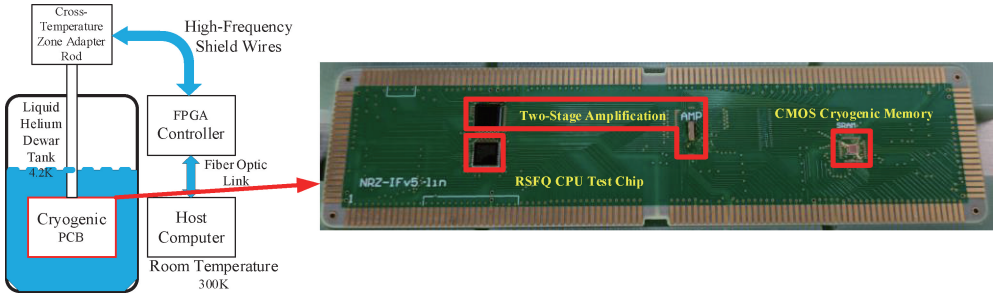


Fig. 11 Overview of the proposed superconducting RSFQ circuit control system

The physical layout of the superconducting RSFQ CPU test chip is shown in Fig. 12. Its working principle is to first read the 8-bit data from address 0 – 511 in the cryogenic memory in turn and then write them to address 512 – 1023 in turn. One working cycle includes 512 read/write operations. The experimental process is as follows: first, the host computer writes 512 bytes of test data into the cryogenic memory at 0 – 511 addresses through the FPGA. Then, the FPGA controls the superconducting RSFQ CPU test chip to start working. After 512 data reading and writing operations in a working cycle, the FPGA controller reads the data of address 512 – 1023 in the cryogenic memory and transmits it back to the host computer. The initial data of address 0 – 511 at the host computer is then compared with the received data to judge whether the superconducting RSFQ CPU test chip is working correctly.

4.2 Demonstration of the control system

The maximum operating frequency of the RSFQ test CPU in the simulation test is 1 GHz. The clock generator's maximum output frequency is 5 GHz, and the operating frequency of the cryogenic memory is also 1 GHz. In the physical test, the superconducting RS-

FQ CPU test chip is driven by a 1 GHz clock generator, and the CMOS cryogenic memory circuit operates at a frequency of 5 MHz. However, due to limitations in the experimental equipment, it is impossible to directly observe the clock output signal of 0.2 mV with a frequency greater than 1 MHz. Therefore, the design of the clock generator and asynchronous communication interface circuit requires validation through checking the results of data read and write operations.

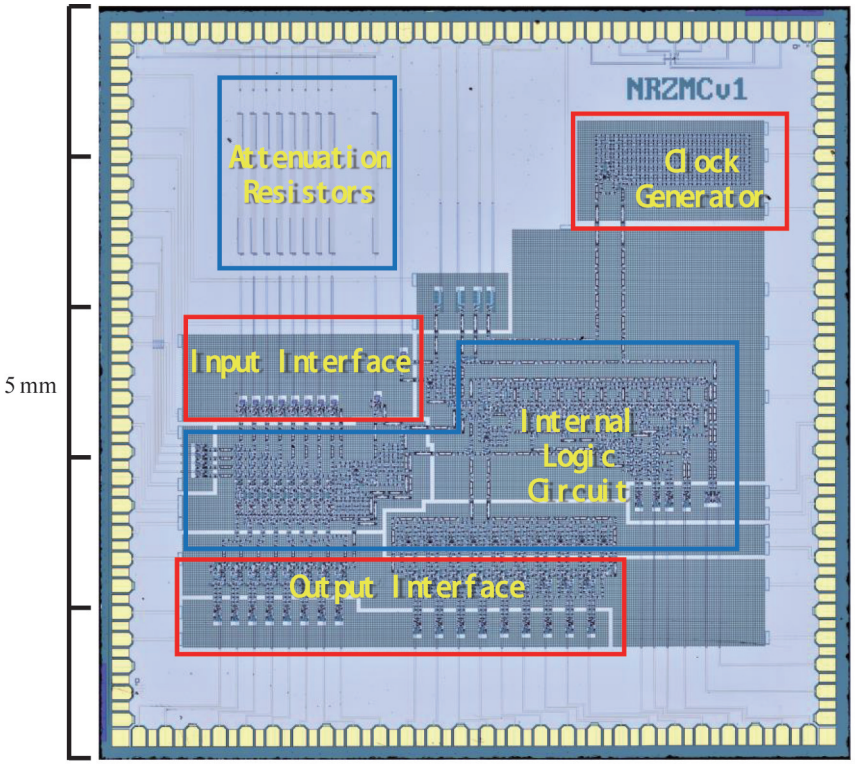


Fig. 12 Superconducting RSFQ CPU test chip physical layout

Validating the entire control system consists of several independent experiments. One such experiment involves writing data to the cryogenic memory by the host computer, which verifies that the connection between the cryogenic system and the room temperature system is reliable. Another experiment involves controlling the superconducting RSFQ CPU test chip to start and stop operation through the FPGA, which can validate the correctness of the clock generator design proposed in this paper. If the superconducting RSFQ CPU test chip can sample the correct pulse signal at the data input port, it can prove the correctness of the input interface circuit design. Similarly, if the data output by the test chip can be written to cryogenic memory, it verifies the correctness of the output interface circuit design.

The series of experiments above can be performed as a complete validation test. The test results of the superconducting RSFQ circuit control system are shown in Fig. 13, which is observed from the FPGA controller.

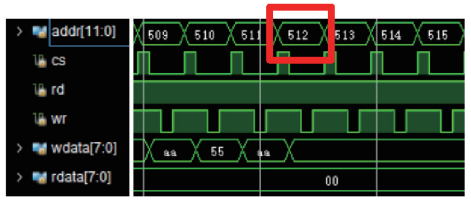
Fig. 13(a) shows that the host computer writes the initial data to the cryogenic memory through the FPGA controller, with memory address 0 – 511 being alternately written with '55' and 'aa', while the address 512 – 1023 is written to '0'. Fig. 13(b) validates the written data by reading all the cryogenic memory out, indicating that the FPGA controller's read/write function of the cryogenic memory is correct.

Subsequently, the FPGA controls the superconducting RSFQ CPU to begin work. After the CPU test chip completes its computation, the FPGA controller reads the data in the memory again, with the reading result shown in Fig. 13(c). The data written by the superconducting RSFQ CPU is located at address 512 – 1023 of the cryogenic memory, and Fig. 13(c) shows that the data at address 512 – 1023 is the same as the data at address 0 – 511.

The whole superconducting RSFQ circuit control system works correctly in the reading and writing tests, which proves the feasibility and effectiveness of the control system design proposed in this paper.

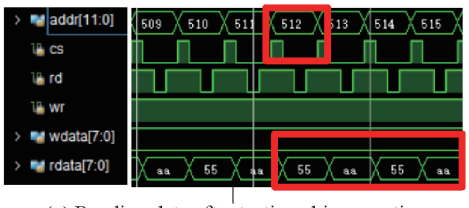
5 Conclusion

This article proposes a design for a superconducting RSFQ circuit control system that utilizes an asynchronous communication interface circuit and clock generator. The design is validated through a series of experiments, including writing data to the cryogenic memory, controlling the superconducting RSFQ CPU, sampling the input pulse signal, and writing the test chip's output data to cryogenic memory. The testing results demonstrate the correctness of the input/output circuit designs and the effectiveness of the control system overall. The proposed design and testing procedures provide a feasible and effective method for controlling superconducting RSFQ circuits, which can potentially advance the development of future supercomputers.



(a) Writing data to memory

(b) Verifying the correctness of the written data



(c) Reading data after testing chip operation

Fig. 13 Waveform of FPGA controller in the control system verification test

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ZHANG Kuozhong, born in 1992. He has been a Ph. D candidate in Institute of Computing Technology of Chinese Academy of Sciences since 2016. He also received his B. S. degree from Huazhong University of Science and Technology in 2014. His research interests include the superconducting RSFQ computer architecture design.