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Fully-integrated ultra-wide band LNA in 0.18 μm CMOS technology for 3 – 10 GHz applications①

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Abstract

The paper presents a fully integrated ultra-wide band (UWB) low noise amplifier (LNA) for 3 – 10 GHz applications. It employs self-biased resistive-feedback and current-reused technique to achieve wide input matching and low power characteristics. An improved biased architecture is adopted in the second stage to attain a better gain-compensation performance. The design is verified with TSMC standard 1P6M 0.18 μm RF CMOS process. The measurement results show that the parasitic problem of the transistors at high frequencies is solved. A high and flat S_{21} of 9.7 ± 1.5 dB and the lowest NF 3.5 dB are achieved in the desired frequency band. The power consumption is only 7.5 mA under 1.6 V supply. The proposed LNA achieves broadband flat gain, low noise, and high linearity performance simultaneously, allowing it to be used in 3 – 10 GHz UWB applications.

Key words: ultra wide band (UWB), self-biased, current-reused, gain compensation, CMOS low noise amplifer (LNA)

0 Introduction

With the rapid development of wireless communication, the increasing demand for high data rates becomes more urgent. For orthogonal frequency division multiplexing (OFDM) multi-channel system, it needs more bandwidth to meet the requirements of high data rates. Because the crowded spectrum resources limit the expansion of bandwidth in the low-frequency band, high-frequency UWB communication standards have emerged. Since 2002, the FCC has approved UWB technology for civilian use in the frequency range of 3.1 to 10.6 GHz[1], so it inspires more and more researches in recent years.

In the design of a UWB receiver front-end, LNA is a critical block that receives small signals from the whole UWB band (3 – 10 GHz) and amplifies them with a good signal-to-noise ratio property. In the design of UWB LNAs, several topologies have been proposed to satisfy all the requirements. Common-gate (CG) topology which incorporates noise-canceling techniques has been employed for both the wideband input matching and lower noise[1,2]. But it is achieved at the cost of higher power consumption and design complexity. Moreover, the associated noise of the auxiliary stage in noise-canceling path itself deteriorates the input noise figure (NF) of LNA. In Refs[3,4], a resistive feedback multi-stage common-emitter amplifier structure obtains superior broadband performance by exploiting the SiGe HBT process. However, incompatibility with standard CMOS process makes it difficult to be integrated with other modules in the receiver. Another topology of the LNA is cascade common-source (CS) amplifier which uses a Chebyshev input matching filter to achieve a well wideband and a high power gain characteristic[5]. But NF is degraded by the insertion loss of the filter. Refs[6,7] utilizes a body biasing technique to decrease the threshold voltage of the transistor, and it solves the voltage headroom limitation in low voltage applications. However, it brings the potential risk of forward conduction between P-type substrate and N-well. Nonetheless, the circuit in the listed references above can't simultaneously meet the characteristics of low power consumption, a smaller chip area, broadband, low NF, etc.

So Refs[8,9] employs a 2-stage resistance shunt-shunt feedback CS topology with the self-biased and current-reused technique in order to get a tradeoff of the low power, wideband and gain property. But its 2nd stage still applies a resistive-feedback structure which will result in the decrease of the gain. To guarantee the sufficient gain, the width of the CS transistor has to be doubled, inevitably causing a more parasitic

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effect.

This paper proposes an improved 2-stage CS structure, in which the 2nd stage adopts an independent voltage biased (IVB) gain-compensation technique. It solves the parasitic problem of the transistors at high frequencies effectively. The design is verified with TSMC standard 1P6M 0.18 μm RF CMOS process. A high and flat S_{21} of 9.7 ± 1.5 dB and the lowest NF 3.5 dB are achieved in the desired frequency band, making it a good candidate for UWB applications.

The paper is organized as follows. Section 1 describes a detailed design of the proposed LNA, including analysis of the output matching performance. In Section 2, measurements result is discussed and comparisons with previous studies is made. Section 3 gives the conclusion.

1 Circuit design

1.1 Circuit structure analysis

Fig. 1 depicts a complete scheme of the proposed UWB LNA, in which the important device parameters are labeled. The LNA is divided into 2 stages. Its 1st stage adopts a resistive-feedback self-biased architecture to achieve a wideband input matching. And transistor M_2 constitutes the 2nd common source stage to obtain a higher gain. Since the circuit also uses a current-reuse technique, no additional driving current is needed for the input stage. Source degeneration inductor L_2 is chosen to reduce the NF and match to the input impedance[10]. Peaking inductor L_3 creates a self-bias current path. Other inductors and capacitors are primarily used for input and output matching, as well as inter-stage matching. Both the 2 stages employ an inductive peaking technology to expand the bandwidth.

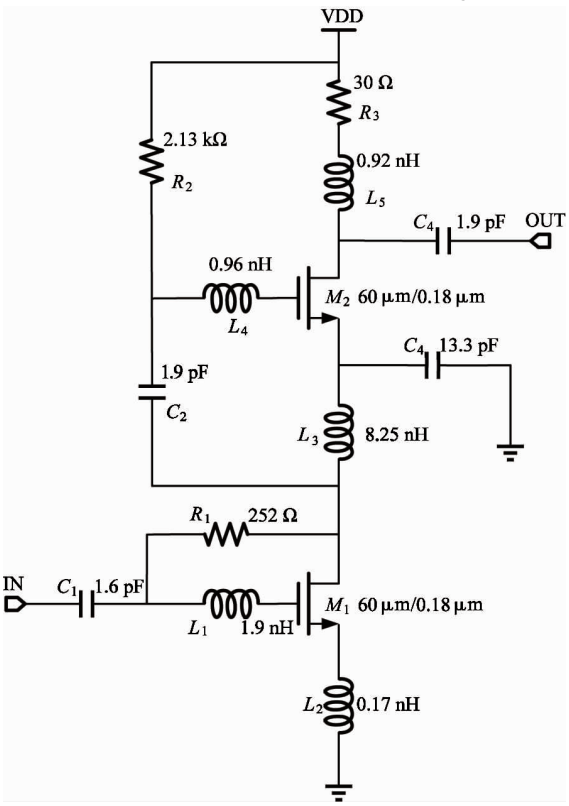

Fig. 1 Schematic of the proposed UWB LNA

As shown in Fig. 1, compared with the conventional circuit[8], the 2nd gain stage uses an IVB structure instead of the resistive-feedback self-biased topology, which makes it have a higher gain-compensation performance. Therefore, the width to length (W/L) ratio of the transistor can be reduced drastically. It strongly decreases the parasitic effect of transistor M_2. For instance, if a transistor W/L ratio of a few hundred is taken, the gate-drain parasitic capacitance C_{gd} can't be ignored. It will decrease the amplificatory ability of the transistor at the high-frequency application. With the IVB topology, a lower W/L ratio CS structure can be employed in the design.

In addition, since the 2nd stage employs a higher gain compensation structure, it also relieves the pressure of the 1st gain stage so that it can utilize a smaller feedback resistor to obtain a wider low-frequency bandwidth[11], reducing the contribution of thermal noise to the LNA. Moreover, inductor L_4 is also added to the gate terminal of M_2 to push the high-frequency poles outside of the 3 – 10 GHz band of interest, which guarantees the bandwidth of output high-frequency band. Furthermore, L_4 and C_{gd2} form series resonance high resistance to the signal simultaneously. Therefore, it effectively prevents the high-frequency input signal from being forward-passed and output signal from being reverse-leaked. When C_{gd2} takes an estimated value of 100 fF, the wideband resonance impedance can reach up to the order of kilo ohms.

1.2 Output impedance analysis

To facilitate the impedance analysis of the proposed LNA, the corresponding small signal equivalent circuit is presented, as shown in Fig. 2. Since the circuit operates at high frequencies, the Miller effect of the transistor cannot be ignored. Resistor R_3 in series with the output peaking inductor L_5 broadens the frequency band by introducing one transmission zero.

To further verify the matching effect of R_3, the output impedance equivalent circuit is shown in Fig. 3, where C_{gd2} is replaced by output equivalent miller capacitor.

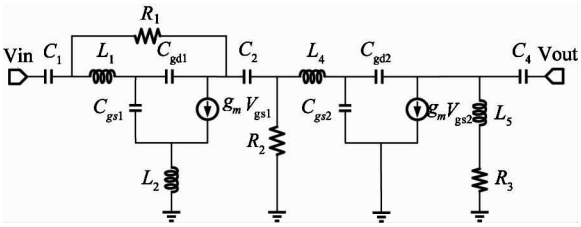

Fig. 2 Small signal equivalent circuit of the proposed LNA

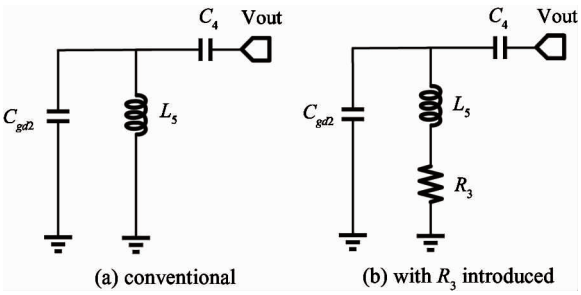

Fig. 3 Equivalent circuit of output impedance

For Fig. 3(a), the output Z_{out} expression is shown as follows:

$$Z_{out} = \frac{1}{sC_4} + sL_5 // \left(\frac{1}{sC_{gd2}}\right) = \frac{1}{sC_4} + \frac{sL_5}{1 + s^2 L_5 C_{gd2}} \quad (1)$$

where s represents the Laplace operator. Substituting $s = j\omega$, thus:

$$Z_{out} = \frac{(1 - \omega^2 L_5 C_{gd2}) - \omega^2 L_5 C_4}{j\omega(C_4 - C_4 L_5 C_{gd2})} \quad (2)$$

From Eq. (2), Z_{out} only contains the imaginary part.

For Fig. 3(b), by introducing R_3, the output expression is

$$Z_{out} = \frac{1}{sC_4} + (sL_5 + R_3) // \left(\frac{1}{sC_{gd2}}\right) = \frac{1}{sC_4} + \frac{sL_5 + R_3}{1 + s^2 L_5 C_{gd2} + sC_{gd2} R_3} \quad (3)$$

For $s = j\omega$, Eq. (4) can be obtaind:

$$Z_{out} = \frac{1 - (C_{gd2} L_5 + L_5 C_4)\omega^2 + j\omega(C_{gd2} + C_4) R_3}{-\omega^2 C_4 C_{gd2} R_3 + j\omega(C_4 - \omega^2 C_4 C_{gd2} L_5)} \quad (4)$$

Thus,

$$Re(Z_{out}) = \frac{R_3 \omega^2 C_4^2}{(\omega^2 C_4 C_{gd2} R_3)^2 + (\omega C_4 - \omega^3 C_4 C_{gd2} L_5)^2} = \frac{R_3}{(\omega C_{gd2} R_3)^2 + (1 - \omega^2 C_{gd2} L_5)^2} \quad (5)$$

Eq. (5) shows that the introduction of resistor R_3 can achieve real impedance. It provides us a convenient adjustment degree of freedom for output impedance matching.

2 Measurement results

The prototype chip is fabricated with the TSMC 0.18 μm RF CMOS process. The photograph of the designed LNA is shown in Fig. 4. The area of the die, including the pads, is 0.73×0.97 mm^2, and the current consumption is 7.5 mA with a 1.6 V supply voltage. The chip is tested via on-wafer probing. The measurements are carried out with an Agilent E8363B vector network analyzer, an E4448A spectrum analyzer and an N8975A noise figure analyzer.

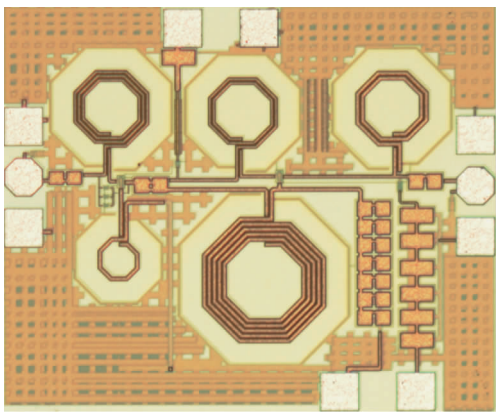

Fig. 4 Die photograph

Fig. 5 gives the S parameter of the circuit. The forward gain (S_{21}) is 9.7 dB from 3 to 10 GHz with the gain flatness of ±1.5 dB. The input return loss (S_{11}) is less than −10 dB from 2 to 10 GHz. Fig. 6 shows that the output return loss (S_{22}) is typically less than −10 dB and the reverse isolation (S_{12}) is less than −27 dB respectively.

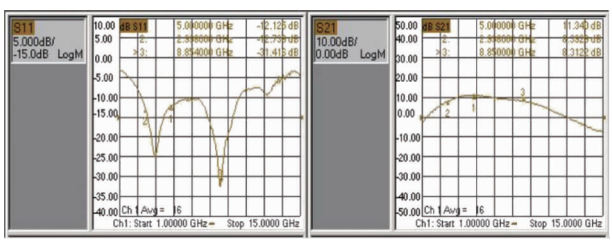

Fig. 5 Measured S-parameters S_{11} and S_{21}

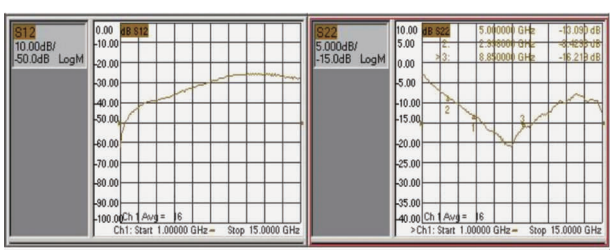

Fig. 6 Measured S-parameters S_{12} and S_{22}

The measured NF curve is shown in Fig. 7. The NF is lower than 5.6 dB in the desired band and the average value is about 4.55 dB (lowest 3.525 dB at 7.4 GHz).

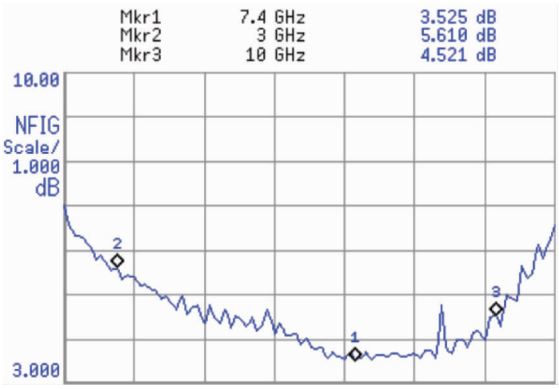

Fig. 7 Noise figure

Fig. 8 illustrates the 2-tone IIP3 test in the frequency domain. The input to the amplifier is 2 sine waves (fundamental) with −14.35 dBm input power, one at 7.0005 GHz and the other at 6.9995 GHz, for which the frequency interval is 1 MHz. Fig. 9 shows the curve-fitting result and it exhibits an −13.76 dBm of input $P_{-1\mathrm{dB}}$, −4.63 dBm of IIP_3 at 7 GHz.

A figure of merit (FOM) suitable for evaluating the performance of a wideband LNA is defined as[12]

$$FoM = \frac{Gain_{mean}(\mathrm{dB}) \times BW(\mathrm{GHz})}{(NF_{mean}(\mathrm{dB}) - 1) \times P_{diss}(\mathrm{mW})} \quad (6)$$

The comparison results with other published work of similar 2-stage CS structure that contains the key parameters are listed in Table 1. It shows that the proposed work achieves the highest FOM, which can meet the requirements of 3 − 10 GHz UWB applications well. Therefore, the proposed LNA achieves good performance in the wide frequency range.

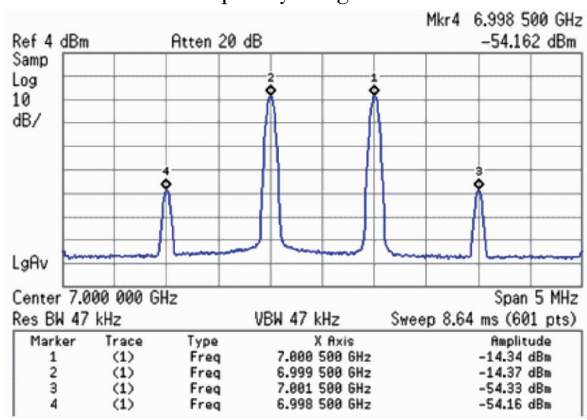

Fig. 8 IIP3 test at frequency 7 GHz

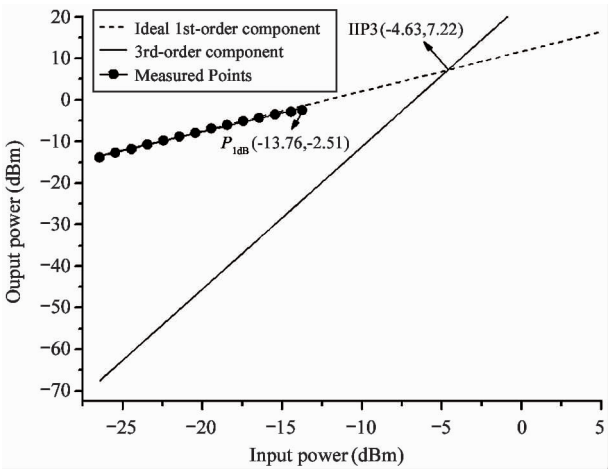

Fig. 9 IIP3 and $P_{-1\mathrm{dB}}$

Table 1 Summary of performance and comparison with state of the art**

Specification	This work	Ref. [11]	Ref. [13]	Ref. [14]	Ref. [15]	Ref. [16]
S_{11} (dB)	< −10	< −11.8	< −9.7	< −9.9	< −5	< −11
S_{22} (dB)	< −10	< −12.6	< −8.4	< −10	< −6	< −10
S_{21} (dB)	9.7 ± 1.5	11.2 ± 2.3	11.4 ± 0.4	9.3	16.7 ± 0.15	9.7
BW(GHz)	3 − 10	1.7 − 5.9	3.1 − 10.6	2.3 − 9.2	3 − 5	1.2 − 11
Average NF(dB)	4.55	4.15	4.64	5.2	3.2	4.8
IIP3(dBm)	−4.67@7 GHz	−12	0.72@6.4 GHz	−6.7@7 GHz	−4@5 GHz	−6.2@7 GHz
Power(mW)	12	10.34	22.7	9	13	20
FoM(GHZ/mW)	1.6	1.4	1.03	0.97	1.17	1.37
Area(mm^2)	0.708	0.565*	0.447*	1.1	/	0.59*

*: Not include the pad, **: Standard 0.18 μm CMOS process

3 Conclusions

This paper presents an improved gain-compensation 2-stage CS UWB LNA with a self-biased, current-reuse technology in 0.18 μm TSMC RF process. The circuit provides a gain of 9.7 dB with the gain flatness of ±1.5 dB in the band of 3 − 10 GHz, and gives an

average 4.55 dB NF in a band of 7 GHz while providing an excellent performance of linearity. The whole circuit consumes only 7.5 mA current from a 1.6 V supply. The excellent performance of the circuit makes itself ideal for ultra-wideband RF receiver front-end applications.

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