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A novel method of optimizing latch comparators①

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Abstract

A new method of improving speed of latch-type comparators with preamplifier is presented. It investigates the relationship of current and transistor scales which affect delay time (tp) in latch. It applies a mathematical model to optimize latch design. A figure of merit indicates that ratio Ipmos/Inmos is 0.25 in latch leading to optimal delay time. In order to suppress offset of latch, the cross-coupled loading, adopted in telescope preamplifier, which enhances the gain, is well analyzed and designed. The chip is fabricated in 0.18 μm CMOS technology. The delay time of latch comparator is less than 400 ps @ 500 MHz. The offset of comparator is estimated through Monte Carlo simulation. And power consumption is only 144 W under 1.8 V power supply. Results of on wafer testing are presented at the end of the paper. The chip occupies an area of 0.66×0.55 mm^2 and drains current of 80 μA.

Key words: cross-couple latch, offset, telescope amplifier with cross-couple loading, delay time

0 Introduction

Comparator is the critical block in analog-to-digital converters (ADC), which is applied to convert analog signal to digital bits. For comparator design, delay time of latch is a critical character, which relates to comparator's speed and accuracy directly. In order to decrease delay time, many work has been done in this area. Some designs employed discharge mode to speed up[1]. In other work[2-4], setting optimal input dc/power supply ratio, or selecting proper device size, could also decrease the delay time. In order to improve delay time of comparators, a novel optimization method is delivered. Through g_m/i_d method, a model of delay time is proposed. Applying mathematical analysis to the parameters in the delay time model, an optimal result is obtained, which is discussed at length in Section 2.

Due to positive feedback loop which amplifies tiny input signal, latch is prevalent in comparator design. However, latch introduces severe offset, which deteriorates performance of comparator greatly. In order to reduce offset voltage, a high gain preamplifier is employed, which feeds current to regenerative cross-coupled pairs. In addition, a small size transistor leads to severe mismatch, which is produced by wafer process deviation. In previous work, many techniques have been introduced to deal with input referred offset. Although negative feedback block[5] and offset storage calibration block[6] could reduce offset of comparator, the power dissipation and the circuit complexities increase greatly. In this case, trade-off in circuit design is necessary. It is efficient that applying telescope amplifier with cross-coupled active load to achieve high gain in low power consuming, which suppresses input referred offset voltage. Besides, kickback noise[7,8] elimination block, which is a reliable method introduced in previous work, is also indispensable in this work.

All these methods mentioned above intend to improve resolution and decrease delay time of comparator with low power dissipation. This paper is organized as follows: Design considerations are presented in Section 1. Analysis and design of comparator is introduced in Section 2. Section 3 presents simulation results. In Section 4, paper is concluded.

1 Design consideration for comparator

In ADC, a comparator makes decision of analog signals, and exports digital bits. Thus, the ADC performance mainly depends on capacity of comparator,

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and latch, the core of comparator, processes high gain due to two cross-couple pairs in regeneration mode. However, referring to lower power dissipation and smaller scale of transistor, mismatch of latch pairs introduces large input referred offset voltage. In order to suppress offset voltage, applying a high gain preamplifier in front of latch could guarantee the performance of comparator[9].

In pipelined ADC, a digital correction algorithm could rectify comparator offset voltage which is within one interval. Thus, comparator in MDAC must meet the requirement in Eq. (1).

$$\sigma_{offset} < V_{ref} / 2^{N_i} \tag{1}$$

where, V_{ref} indicates differential input range, N_i represents resolution of MDAC per stage.

However, as supply voltage decreases and multiple digital to analog convertor (MDAC) output bits increases, capacity of correction algorithm declines. For 6 bit MDAC, with 1.2 V V_{ref}, the resolution of MDAC is 18.75 mV. Thus, the offset of comparator must be lower than ±9.375 mV. And delay time is less than 0.5 ns.

The structure of the comparator is shown in Fig. 1. The differential telescope circuit is adopted for preamplifier design. M_1, M_2 are input differential pair, with M_{1a} and M_{2a} working as capacitors to absorb kickback noise. In order to enhance preamplifier's gain, cascode structure is a better choice. M_7 and M_8 is cross-coupled load, which improves output gain.

The latch consists of two cross-couple pairs, PMOS M_{11}, M_{12} and NMOS M_{13}, M_{14}, with M_{15} and M_{16} working as reset switch. The two cross-couple pairs provide strong positive feedback to regenerate signals. M_9 and M_{10} could also separate the capacitor loading from the preamplifier.

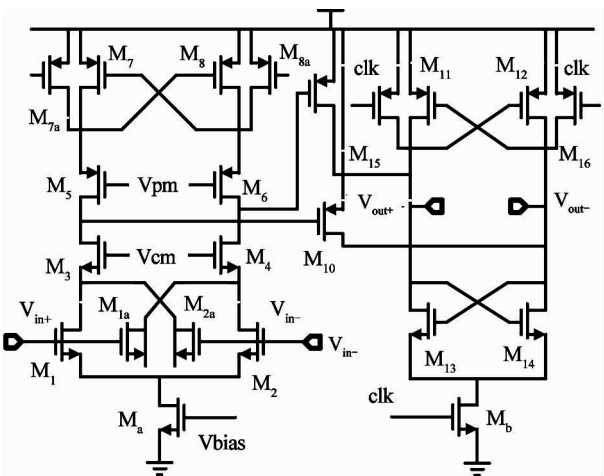

Fig. 1 The structure of preamplifier latch

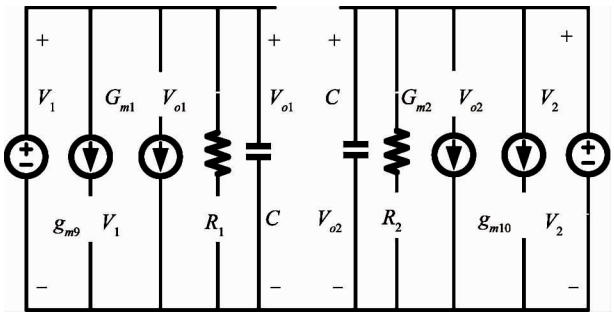

Fig. 2 Small signal model of latch

2 Comparator analyses

2.1 Delay time model

Fig. 2 shows the small signal equivalent circuit of latch, where G_{m1} is the combination of equivalent trans-conductance g_{m11} and g_{m13}, C is the equivalent capacitors at output, R_i is the output resistant loading, V_1 and V_2 are output voltage of preamplifier, g_{m9} and g_{m10} is equivalent trans-conductance of folded part of latch.

Referring to Fig. 2, the KVL expression[10,11] could be stated as Eq. (2).

$$\begin{aligned} g_{m9}V_1 + V_{o2}G_{m1} + V_{o1}/R + C\frac{dV_{o1}}{dt} &= 0 \\ g_{m10}V_1 + V_{o1}G_{m2} + V_{o2}/R + C\frac{dV_{o2}}{dt} &= 0 \end{aligned} \tag{2}$$

Solving Eq. (2), Eq. (3) is obtained.

$$\begin{aligned} V_{o1}(t) = {} & \frac{1}{2}\Bigg[\sqrt{\frac{G_{m1}}{G_{m2}}}\left(V_{o2.0} + \frac{g_{m9}}{G_{m1}}V_{1.0}\right) \\ & + \left(V_{o1.0} + \frac{g_{m10}}{G_{m2}}V_{2.0}\right)\Bigg]\exp\left(-\frac{t}{\tau}\right) - \frac{1}{2} \\ & \Bigg[\sqrt{\frac{G_{m1}}{G_{m2}}}\left(V_{o2.0} + \frac{g_{m9}}{G_{m1}}V_{1.0}\right) \\ & - \left(V_{o1.0} + \frac{g_{m10}}{G_{m2}}V_{2.0}\right)\Bigg]\exp\left(\frac{t}{\tau}\right) - \frac{g_{m10}}{G_{m2}}V_2 \\ V_{o2}(t) = {} & \frac{1}{2\sqrt{\frac{G_{m1}}{G_{m2}}}}\Bigg[\sqrt{\frac{G_{m1}}{G_{m2}}}\left(V_{o2.0} + \frac{g_{m9}}{G_{m2}}V_{1.0}\right) \\ & + \left(V_{o1.0} + \frac{g_{m10}}{G_{m2}}V_{2.0}\right)\Bigg]\exp\left(-\frac{t}{\tau}\right) \\ & + \frac{1}{2\sqrt{\frac{G_{m1}}{G_{m2}}}}\Bigg[\sqrt{\frac{G_{m1}}{G_{m2}}}\left(V_{o2.0} + \frac{g_{m9}}{G_{m2}}V_{1.0}\right) \\ & - \left(V_{o1.0} + \frac{g_{m10}}{G_{m2}}V_{2.0}\right)\Bigg]\exp\left(\frac{t}{\tau}\right) - \frac{g_{m9}}{G_{m1}}V_1 \end{aligned} \tag{3}$$

where τ^2 is $G_{m1}G_{m2}/C_2$, $V_{i.0}$ is initial input voltage, and $V_{oi.0}$ is initial output voltage. Assuming that input differential signal is small enough, differential pairs share equal states. It is concluded from Eq. (3) that:

$$G_{m1} = G_{m2},\ g_{m9} = g_{m10}$$
$$\Delta V_o(t) = V_{o2}(t) - V_{o1}(t)$$
$$= \frac{g_m}{G_m}(V_{1.0} - V_{2.0})\exp(t/\tau) - \frac{g_m}{G_m}(V_1 - V_2) \quad (4)$$

Because $V_{1.0}$ is slightly different from V_1, the equation could be approximately expressed as Eq. (5).

$$\Delta V_o(t) = \frac{g_m}{G_m}\Delta V_i[\exp(t_p/\tau) - 1] \quad (5)$$

Solving Eq. (5), to could be expressed as Eq. (6).

$$t_p = \frac{C}{G_m}\mathrm{In}\left(\frac{V_{OH} - V_{OL}}{2\Delta V_i}\frac{G_m}{g_m} + 1\right) \quad (6)$$

As mentioned above:

$G_m = g_{m11} + g_{m13}$, $C = C_{gs14} + C_{gs12} + C_{load} + C_{db11} + C_{db13} + C_{db9}$, t_p is mainly determined by C/G_m and G_m/g_m.

2.2 G_m/g_m parameter analysis

Because current through M_{13} is equal to the sum of current from M_{11} and M_9, thus, it is assumed that current from M_{13} is I, and the one from M_{11} is βI. In this case, G_m/g_m could be expressed as

$$\frac{G_m}{g_m} = \frac{I/vov_{13} + \beta I/vov_{11}}{(1-\beta)I/vov_9} \approx \frac{\dfrac{1}{vov_{13}} + \dfrac{\beta}{1.8 - (V_{thn} + |V_{thp}|) - vov_{13}}}{\dfrac{1-\beta}{vov_9}} \quad (7)$$

The partial derivative of G_m/g_m to β is expressed as

$$\partial\frac{\frac{G_m}{g_m}}{\partial\beta}\Big|_{vov13 = vov9} = \frac{2}{(1+\beta)^2} \quad (8)$$

From Eq. (8), the derivation of G_m/g_m is always positive. As a result, G_m/g_m decreases with β decreasing. However, considering the size of transistor and the power consumption of circuit, β ranges from 0.2 to 0.6.

The partial derivative of G_m/g_m to vov_{13} is

$$\partial\frac{\frac{G_m}{g_m}}{\partial vov_{13}} = \frac{-\dfrac{1}{vov_{13}^2} + \dfrac{\beta}{(1.8 - (V_{thn} + |V_{thp}|) - vov_{13})^2}}{\dfrac{1-\beta}{vov_9}} \quad (9)$$

$$vov_{13} = \frac{1.8 - V_{thn} - |V_{thp}|}{1 + \sqrt{\beta}} \quad (10)$$

When $vov_{13} = (1.8 - v_{thn} - |v_{thp}|)/(1 + \beta^{0.5})$, G_m/g_m reaches its minimum value.

In order to have an intuitive view on the effects of two parameters, vov_{13} and β, simulation of G_m/g_m in Matlab is presented in Fig. 3.

As shown in Fig. 3, for a given value of β, together with changing of vov_{13}, G_m/g_m obsesses a minimum value. As a result, G_m/g_m has a series of minimum values, which are presented in Fig. 4. According to Fig. 3 and Fig. 4, it is concluded that picking optimal β, together with related vov_{13}, G_m/g_m could reach the optimal value.

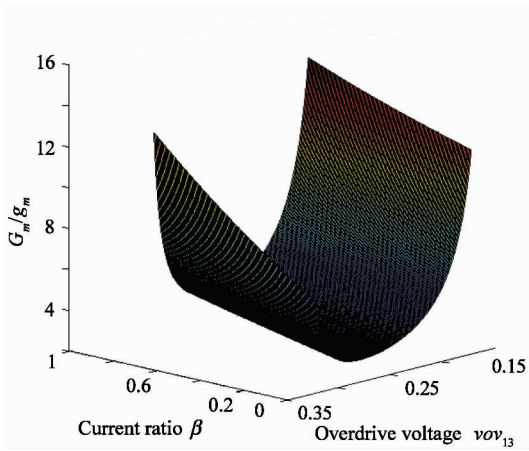

Fig. 3 The simulation curve of G_m/g_m in Matlab

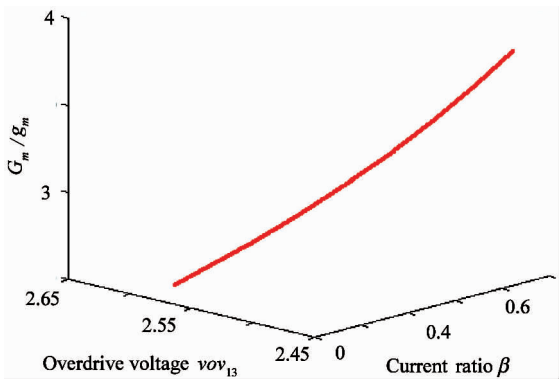

Fig. 4 The minimum value of G_m/g_m in Matlab

As analyzing above, with β getting smaller, the value of G_m/g_m is becoming smaller. Although the minimum value of G_m/g_m could be obtained mathematically, considering scale of transistor for PMOS in wafer process, β could not reach the least value. Trade-off in circuit design is necessary.

2.3 C/G_m parameter analysis

Because the diffusion capacitances, C_{sb} and C_{db}, are not as large as gate capacitance C_{gs} [12], the loading capacitance is expressed in Eq. (11).

$$C = C_{gs14} + C_{gs12} + C_{db11} + C_{db13} + C_{db9} + C_{load} \approx \gamma(C_{gs11} + C_{gs13}) \quad (11)$$

$$\gamma(C_{gs11}+C_{gs13})=\gamma\frac{2}{3}LC_{ox}(w_{pmos-11}+w_{nmos-13}) \tag{12}$$

As mentioned above, it is picked:

$$vov_{13}=\frac{1.8-V_{thn}-|V_{thp}|}{1+\sqrt{\beta}} \tag{13}$$

$$vov_{11}=\frac{\sqrt{\beta}}{1+\sqrt{\beta}}(1.8-V_{thn}-|V_{thp}|) \tag{14}$$

Consider the current relationship between I_{M11} and I_{M13}:

$$\frac{w_{nmos-13}}{L}\mu_n vov_{13}^2=\beta\frac{w_{pmos-11}}{L}\mu_p vov_{11}^2 \tag{15}$$

$$\frac{w_{nmos-13}}{w_{pmos-11}}=\beta^2\mu_p/\mu_n \tag{16}$$

Substituting Eq. (16) to Eq. (12):

$$C=\gamma\frac{2}{3}LC_{ox}w_{pmos-11}(1+\beta^2\mu_p/\mu_n) \tag{17}$$

The G_m could be expressed as

$$G_m=\frac{4I}{1.8-V_{thn}-|V_{thp}|}(1+\sqrt{\beta})^2 \tag{18}$$

Also, I could be expressed as Eq. (19).

$$I=\frac{1}{2}C_{ox}\frac{\omega_{pmos-11}}{L}\mu_p(1.8-V_{thn}-|V_{thp}|)/(1+\sqrt{\beta})^2 \tag{19}$$

From Eqs(17), (18) and (19), it is concluded that:

$$\frac{C}{G_m}=\frac{\gamma L^2C_{ox}(1+\beta^2\frac{\mu_p}{\mu_n})}{3\mu_p(1.8-V_{thn}-|V_{thp}|)} \tag{20}$$

As shown in Eq. (20), C/G_m is nearly proportional to β^2.

Based on the analyses above, current ratio β which affects G_m/g_m and C/G_m in the same trends, is the critical parameter in latch design, which relates to the current drawn from source to latch pairs. Besides, vov_{13} also affects the performance of comparator. In this case, a suitable overdrive voltage for the latch is necessary.

Fig. 5 shows that delay time t_p decreases with β changing. According to the simulation results, smaller β is, faster the delay time will be. As shown in Eq. (20), C/G_m is nearly proportional to β^2.

The simulation result matches the analysis well. Although the minimum value of t_p could be concluded mathematically, which is related to β and vov_{13}, trade-off should be made between power dissipation and transistor scale. Considering the analysis all above, in this work, $\beta=0.25$ and $vov_{13}=0.25$ V are taken.

2.4 Preamplifier design

Preamplifier is separated from latch block, its high gain will substantially decrease the input referred offset introduced by latch.

$$\sigma_{tot}^2=\sigma_{preamp}^2+\sigma_{latch}^2/A_{preamp}^2 \tag{21}$$

In this paper, telescope structure with cross-couple loading amplifier is adopted, which introduces high gain to suppress the offset[13] caused by latch.

The gain of traditional telescope amplifier is

$$A_0=g_{m1}(g_{m3}r_{o3}r_{o1})//(g_{m5}r_{o5}R_{o7}) \tag{22}$$

Small signal model of cross-couple load is shown in Fig. 6. After analyzing, equivalent resistance R_{o7} could be obtained:

$$R_{o7}=\frac{1}{g_{m7a}-g_{m7}} \tag{23}$$

Thus, substituting Eq. (23) to Eq. (22):

$$A_0=g_{m1}(g_{m3}r_{o3}r_{o1})//(g_{m5}r_{o5}\frac{1}{g_{m7a}-g_{m7}}) \tag{24}$$

Pick $W_{7a}/W_7=0.6/0.4$, $g_{m7a}-g_{m7}=0.5g_{m7}$. In this way, gain is enhanced to nearly $(g_m r_o)^2$.

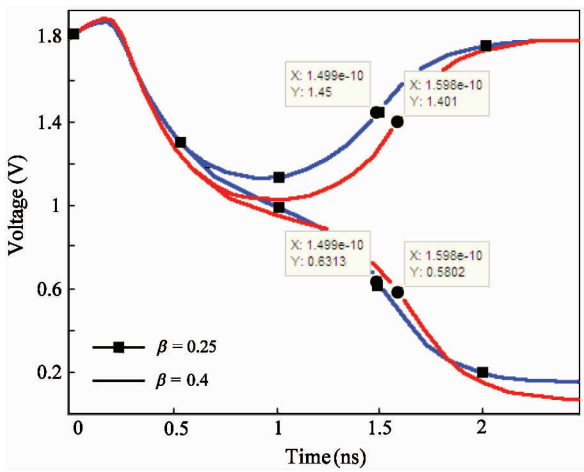

Fig. 5 Delay time for different β

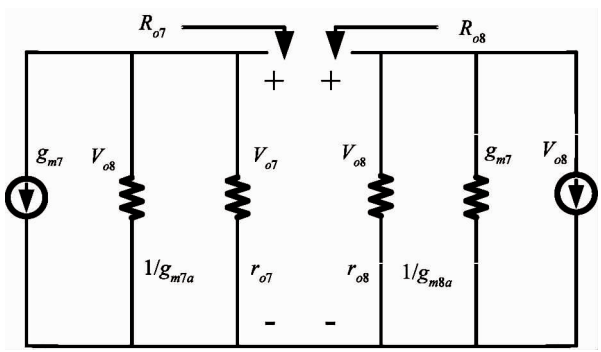

Fig. 6 Small signal model of cross-couple loading

2.5 Kickback noise

The noise and the voltage disturbance could be coupled to the input nodes through the parasitic capacitance of transistors. Adding two transistors M_{1a}, M_{2a} at the input node, with drain and source connected to-

gether, could cancel kickback noise[14], as shown in Fig. 1. And the scale of kickback neutralized transistor must meet the requirement:

$$C_{gd1.2} = \frac{1}{2} C_{ox} W_{1.2} L_{1.2} \tag{25}$$

$$C_{1a.2a} = C_{ox} W_{1a.2a} L_{1a.2a}$$

From Eq. (25), $W_{1a,2a} = 0.5 W_{1,2}$ could be derived.

3 Simulation results

All the simulations have been performed in Cadence, under 0.18 μm CMOS process. The results are showed below.

3.1 Simulation result of preamplifier

Fig. 7 shows the amplitude-frequency characteristic of preamplifier. The 3 dB bandwidth of preamplifier is 325 MHz and DC gain is 26.59 dB, phase margin is 75 degree.

3.2 Pre-simulation of delay time

Fig. 8 shows simulation result of delay time. The clock works at 500 MHz and common-mode voltage equals 1 V. As the simulation result represents, delay time of comparator is 150 ps.

And, the layout of proposed comparator is presented in Fig. 9.

3.3 Post simulation of delay time

The clock in post simulation also works at 500 MHz and input differential voltage equals 1 mV. According to the post simulation results in Fig. 10, delay time of comparator is 300 ps.

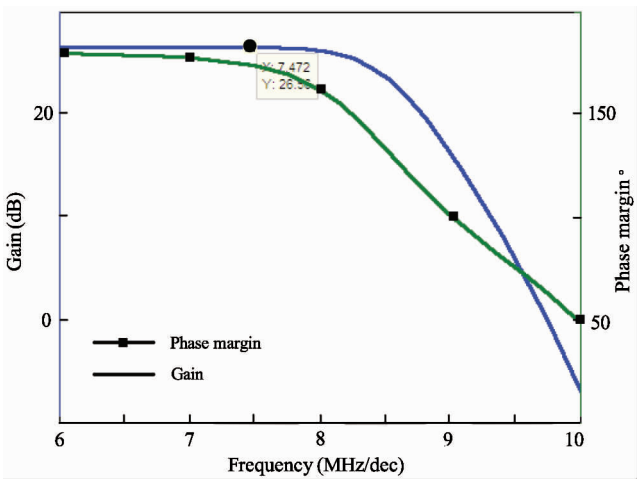

Fig. 7 Amplitude frequency character

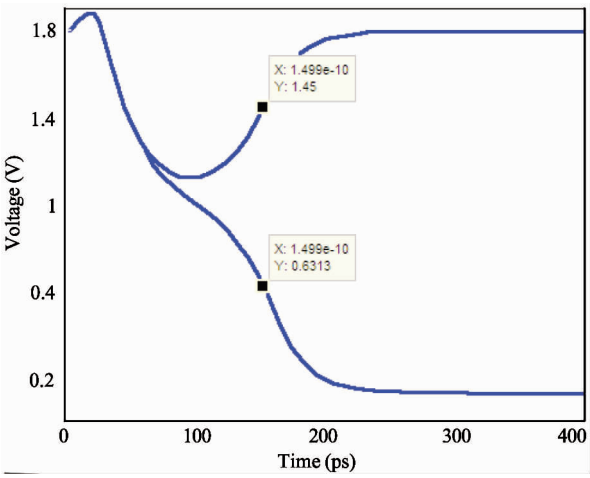

Fig. 8 Delay time with 500 MHz clock

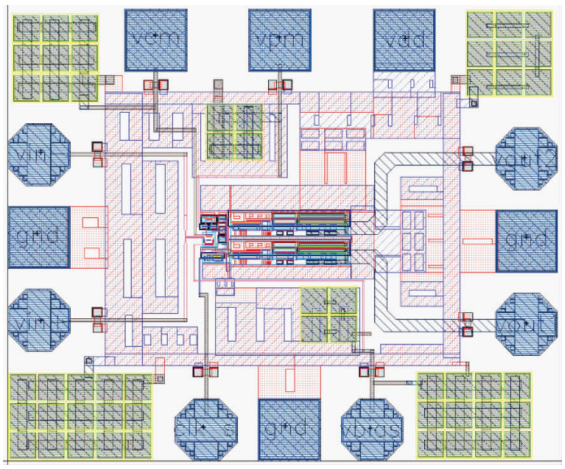

Fig. 9 The layout of the comparator

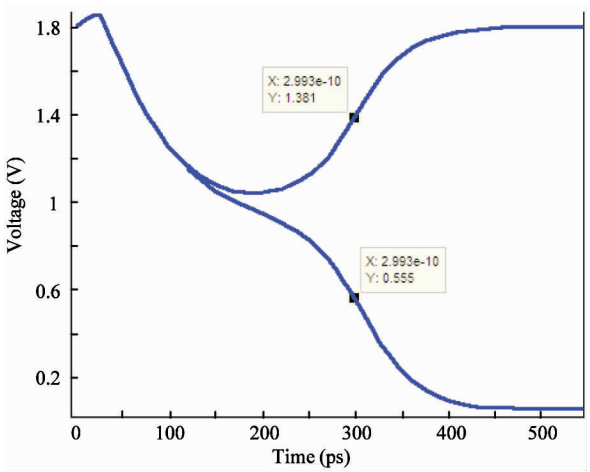

Fig. 10 Post simulation of delay time with 500 MHz clock

3.4 Monte Carlo simulation for input referred offset

The Monte Carlo simulation is presented in Fig. 11. The simulation repeats Monte Carlo for 100 times with transistors variation. As Fig. 11 shows, the

input offset voltage equals to 7 mV.

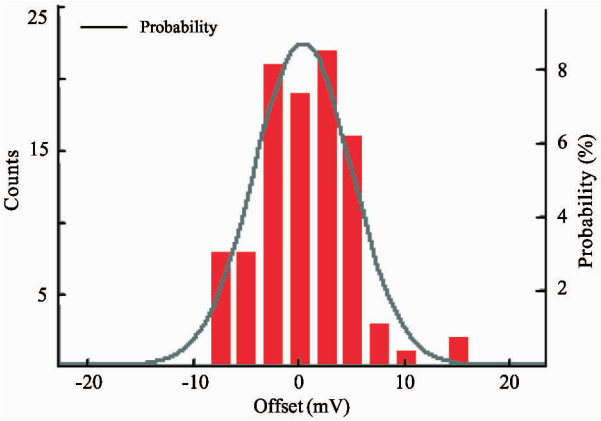

Fig. 11 The Monte Carlo simulation for comparator

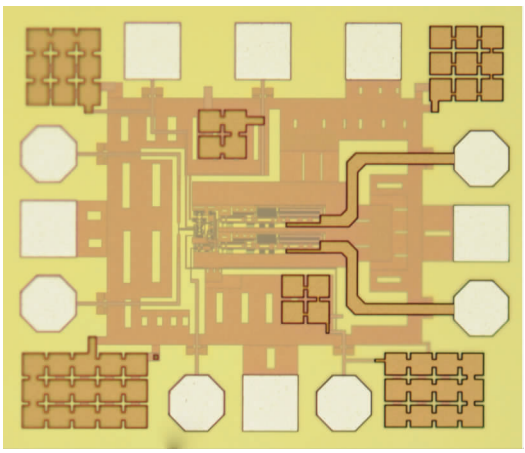

Fig. 12 Chip photograph of comparator

The output waveform is measured through Tektronix MSO 71254C Mixed Signal Oscilloscope. Considering large capacitor loading of oscilloscope, 14 pF capacitor, the comparator applies 5 stage buffers to pull up the output power.

During testing, the input differential signal ranges from 1 mV to 13 mV with the clock working at 500 MHz.

Fig. 13 presents the differential output waveform of comparator with 4mV differential input. And Fig. 14 shows the output waveform with 7 mV input differential signals.

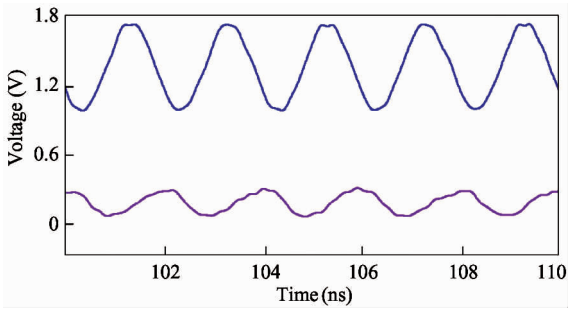

Fig. 13 Differential output with 4 mV input

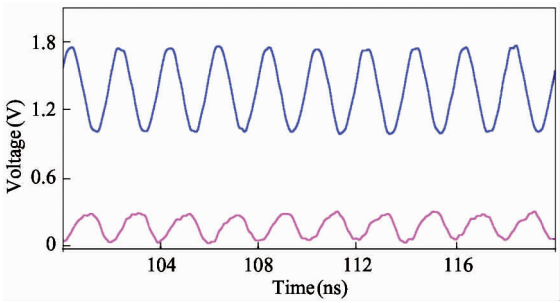

Fig. 14 Differential output with 7 mV input

According to the simulation results above, logic of output waveform is correct. As input increasing, the output waveform becomes more stable. And, the bottom of output waveform is aligned precisely to the peak.

Although bottom and peak of output are separated obviously, the waveforms are not symmetric. Because the output of comparator is powered by multiple stages of buffer to drive oscilloscope, the short slice of clock limits the process of charging and discharging. And buffer's output waveform is not symmetric. Both of these problems lead to the asymmetric measurement results.

Moreover, because time constants of charging and discharging in the oscilloscope are greater than delay time, the delay time of comparator could not be measured precisely. However, it can be observed from testing results that the delay time of comparator is less than 400 ps, which is also in line with the post simulation result.

Table 1 Performance comparison of comparators

Parameter	Comparator[15]	Comparator[10]	This work
Process	0.18 μm CMOS	0.18 μm CMOS	0.18 μm CMOS
Sampling clock	500 MHz	200 MHz	500 MHz
Structure	Latch	Preamplifier	Preamplifier
Power dissipation	329 μW	--	144 μW
Delay time	550 ps	3.5 ns	380 ps
Offser voltage	7.8 mV	0.86 mV	7 mV

The testing results state that comparator is working functionally right, with smaller offset voltage, nearly 4 mV. However, virtually, process parameters, whose deviation obeys Gauss law, are varied during fabricating. Under this circumstances, only measurements of hundred chips could indicate the real offset voltage. So, the Monte Carlo simulation of offset is still convincable.

4 Conclusion

This paper presents a high speed and accurate preamplifier latch comparator. The structure of comparator is analyzed in detail. In order to optimize latch comparator, a novel model is proposed, whose analysis is delivered in mathematical way. The relationship between current and over drive voltage of transistor is discussed thoroughly. In this case, trade-off for mathematical analysis and circuit design is made. In chip testing, delay time of comparator is less than 400 ps. And comparator works stable if input voltage is larger than 4 mV. Compared with other work, Table 1 shows that this work has better performance with high speed and low power dissipation.

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