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A single-ended wideband reconfigurable receiver front-end for multi-mode multi-standard applications in 0.18 μm CMOS①

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Abstract

This paper presents a reconfigurable RF front-end for multi-mode multi-standard (MMMS) applications. The designed RF front-end is fabricated in 0.18 μm RF CMOS technology. The low noise characteristic is achieved by the noise canceling technique while the bandwidth is enhanced by gate inductive peaking technique. Measurement results show that, while the input frequency ranges from 100 MHz to 2.9 GHz, the proposed reconfigurable RF front-end achieves a controllable voltage conversion gain (VCG) from 18 dB to 39 dB. The measured maximum input third intercept point (IIP3) is −4.9 dBm and the minimum noise figure (NF) is 4.6 dB. The consumed current ranges from 16 mA to 26.5 mA from a 1.8 V supply voltage. The chip occupies an area of 1.17 mm^2 including pads.

Key words: reconfigurable, multi-mode multi-standard (MMMS), receiver front-end, gate inductive peaking, noise canceling, CMOS

0 Introduction

The exploding growth of wireless multi-mode multi-standard (MMMS) communication markets urgently requires mobile handsets to have high flexibility of reconfiguration with low power consumption and low cost[1]. Considering the large-dynamic-range signals received by the antenna, the gain variation of the radio frequency (RF) front-end will enhance receiver's capability to deal with larger-dynamic-range signals[2].

Some MMMS front-ends have been reported[3-6]. However, these works focus on wideband and anti-interference, the gain cannot be reconfigurable. Taking LTE for example, the received signal power is changed from −106.2 dBm to −25 dBm. Assuming the gain of RF front-end is fixed to 40 dB, the front-end may be saturated when receiving a larger signal. Thus, when the input signal is strong, low gain or even no gain is needed to avoid the baseband analog circuits saturated, which results in a high noise figure (NF). But the high NF will not corrupt the quality of signal because the power of signal is strong. On the other hand, high gain mode can provide enough gain for small input signals and the RF front-end can also suppress the noise of the following baseband circuits. Another advantage is that power efficiency is improved as a result of the dynamic power consumption according to the received signal level at the antenna. Consequently, a receiver front-end with a reconfigurable gain will definitely be beneficial in achieving the best compromise between linearity, NF and power consumption when receiving MMMS larger-dynamic-range signals.

This paper proposes a novel reconfigurable receiver front-end by employing gate inductive peaking technique. And the digitally-controllable gain achieves a more efficient front-end and wider working frequency.

1 Reconfigurable front-end architecture

The proposed reconfigurable receiver, as shown in Fig. 1, is zero intermediate frequency (IF) architecture to support multiple standards across multiple frequency bands. In this architecture, the receiver's RF front-end is shared among different modes and can be reconfigured flexibly according to received signals.

Single-ended input wideband low noise amplifier (LNA) that is used to save off-chip devices and without baluns can reduce insertion loss to improve noise performance. The LNA has two gain modes and the low

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noise characteristic is achieved by the noise canceling technique while the bandwidth is enhanced by gate inductive peaking technique under high gain mode. On the other hand, differential signal in the receive chain is preferred in order to reduce second-order distortion and reject power supply and substrate noise. Thus single end to differential (S2D) circuit is needed to cascade LNA and the IQ mixer. The reconfigurable quadrature passive mixer has 4 gain modes by using controllable transconductor and transimpedance-amplifier stages. Therefore the RF front-end has 8 different voltage conversion gain (VCG) to satisfy the needs of different wireless communication standards.

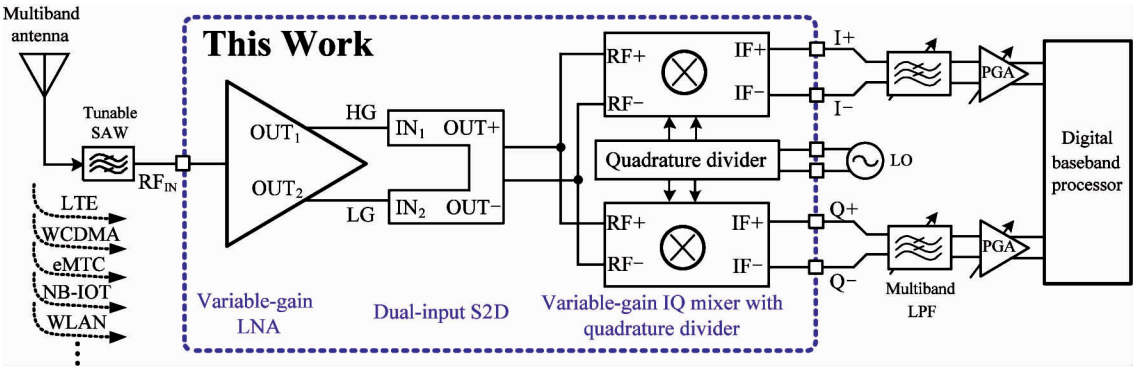

Fig. 1 Block diagram of the proposed MMMS receiver

2 Circuit design

2.1 Wideband LNA with dual inputs S2D

The well-known Bruccoleri's noise canceling technique is efficient to design wideband LNAs since it can break the tradeoff between input matching and NF[7]. Fig. 2 demonstrates the proposed LNA. The matching amplifier stage consists of transistors M_{1a} and M_{1b} with a large capacitor C_1 = 12 pf grounding the source of M_{1b}. The matching stage is AC coupled to M_{sf} via the high-pass filter formed by R_c and C_c. The cascode transistor M_{2b} improves isolation and decreases the Miller effect from M_{2a}. The current bleeding technique is used to provide additional bias current by M_4 for the voltage-sensing amplifier. So it can be tuned to high gain without increasing the DC current of the source follower M_{sf}. The channel thermal noise of the matching devices M_{1a} and M_{1b}, which are the dominant noise component, can be canceled by auxiliary voltage-sensing amplifier at OUT_1 while adding signal contribution.

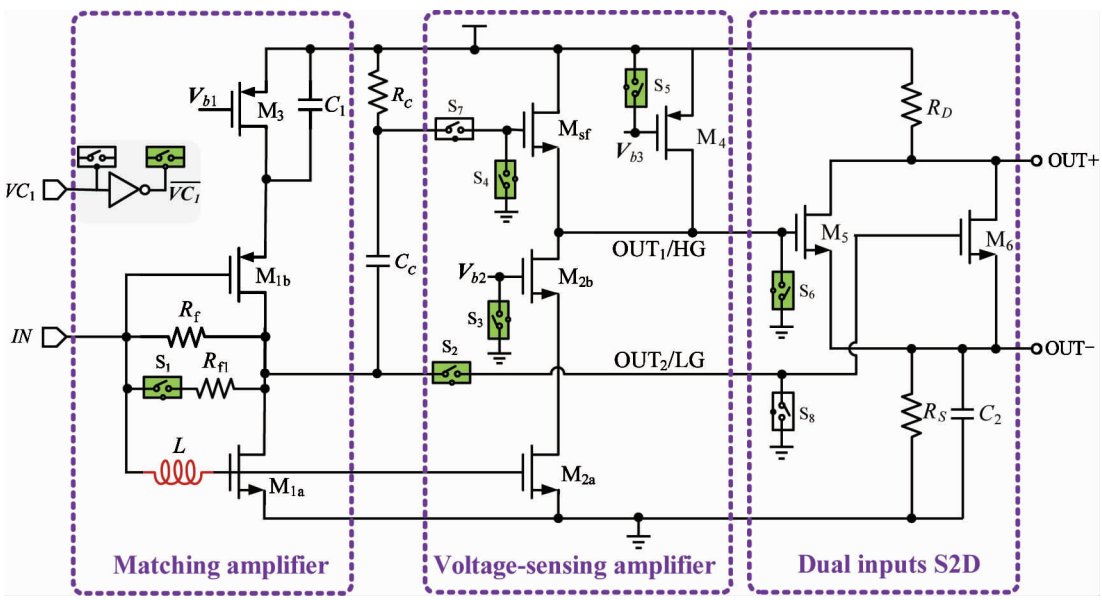

Fig. 2 Schematic of gain-reconfigurable LNA with dual inputs S2D

However, parasitic capacitances can degrade the gain of the amplifier at high frequency, which consequently degrades the high-frequency noise performance. Fig. 2 shows a gate inductor L which is used to

extend the bandwidth of the matching amplifier stage and the voltage-sensing amplifier stage simultaneously. The proposed gate inductive peaking technique splits the poles of the two stages and pushes the complementary poles to higher frequency. As a result, the bandwidth of the gain is extended and the noise performance at high frequency is improved.

Because only one inductor is exploited in the circuit to extend the bandwidth of both stages, the inductor value should be carefully selected to guarantee that the gain of whole LNA is flat and stable. The inductor value affects bandwidth of the LNA as shown in Fig. 3. In this work, considering the tradeoff between bandwidth and stability, an inductor of 5.8 nH is applied in the proposed circuit. High-frequency noise performance is consequently improved by the flattened gain over the entire operating frequency band at the cost of slightly increased area.

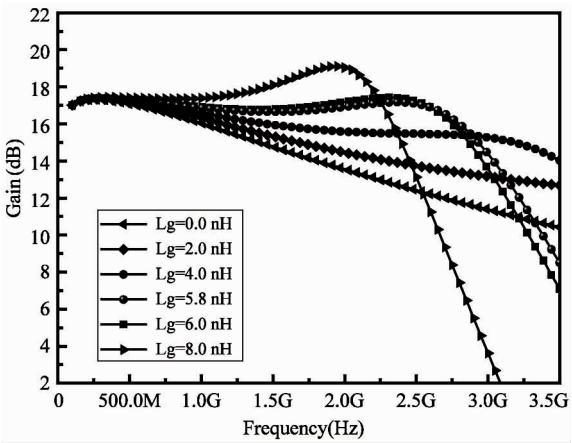

Fig. 3 Simulated gain of LNA with different gate inductors

As discussed above, the gain of LNA should be configured. When VC_1 is high, as shown in Fig. 2, switches $S_1 - S_6$ are off and $S_7 - S_8$ are on, the LNA working at high gain mode and output signal is drawn from OUT_1. When VC_1 is shorted to ground, only matching amplifier stage is working and the output is at OUT_2. In order to further reduce the gain of the first stage, the feedback resistor is changed to parallel R_f and R_{f1}. The effective feedback resistance becomes small and only has a slight influence at matching which is verified by measured results of S_{11} as shown in Fig. 4. But when the voltage-sensing amplifier stage is turned off, the noise of the first stage cannot be cancelled, which means sacrificing the noise performance in exchange of power consumption and increased linearity at the low gain mode.

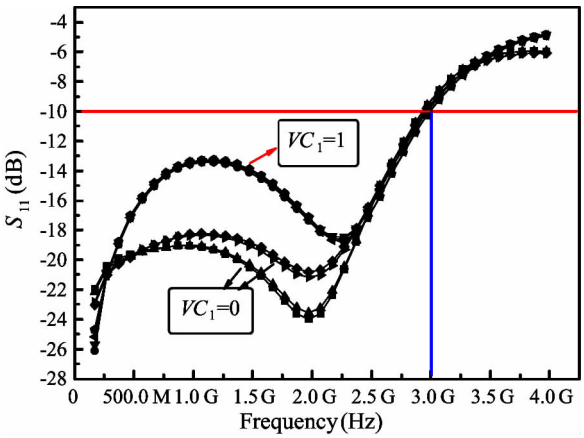

Fig. 4 Measured S_{11} of the proposed front-end with different control words

The output of LNA is the single-end, but the mixer is a fully differential structure. Fig. 2 shows a dual inputs single end to differential (S2D) circuit which connects the LNA high gain and low gain outputs. The common-source common-drain amplifiers produce a balanced differential RF-output. Switches S_6 and S_8 are controlled by the two opposite control words, therefore only one transistor works at a time. Ideally, the output signal at the drain will be phase-shifted by 180° relative to the output signal at the source, with equal amplitude. However, the differential output signals are imbalanced because the drain parasitic capacitances and source parasitic capacitances are not equal. Thus capacitor C_2 is used to balance the drain parasitic capacitances to make the phase of output signals differential.

2.2 Reconfigurable quadrature passive mixer

As illustrated in Fig. 5(a), the IQ reconfigurable passive mixer includes identical I and Q branch. Each branch is composed of a G_m (transconductance) stage, a switching stage, and a TIA (transimpedance-amplifier) stage. The G_m stage converts the input RF voltage signal into an RF current signal which is coupled to the switching stage via C_{C1} and C_{C2} and then is downconverted into an IF current. Afterwards, TIA transforms current signal to voltage signal through the feedback resistor (R_{TIA}) at output and provides first-order low-pass characteristic for the further interference attenuation. To fulfill the performance of reconfiguration, a 2-bit digital control word (VC_2, VC_3) is utilized to control the transconductance of the G_m stage and the transimpedance of the TIA stage. Hence, the VCG of the mixer is derived as

$$VCG_{\text{mixer}} = \frac{2}{\pi} \cdot G_m(VC_2) R_{\text{TIA}}(VC_3) \quad (1)$$

where G_m (VC_2) is the transconductance of the G_m stage, R_{TIA} (VC_3) is transimpedance of the TIA stage, and the coefficient $2/\pi$ is caused by the commutation behavior of switching stage. Therefore VCG has 4 modes corresponding to 4 combinations of VC_2 and VC_3.

The reconfigurable transconductor is a combination of a fixed transconductor Gm_1 and a VC_2-controlled transconductor Gm_2 as shown in Fig. 5(b). Self-biased inverters are employed as the transconductors to save the circuitry of DC bias. When control voltage VC_2 is high, Gm_2 works actively and the effective transconductance is the sum of Gm_1 and Gm_2. On the other hand, no current flows through Gm_2 and the transconductance is provided by Gm_1 alone. In the meantime, the power efficiency is improved because current is partly cut off when low gain is needed.

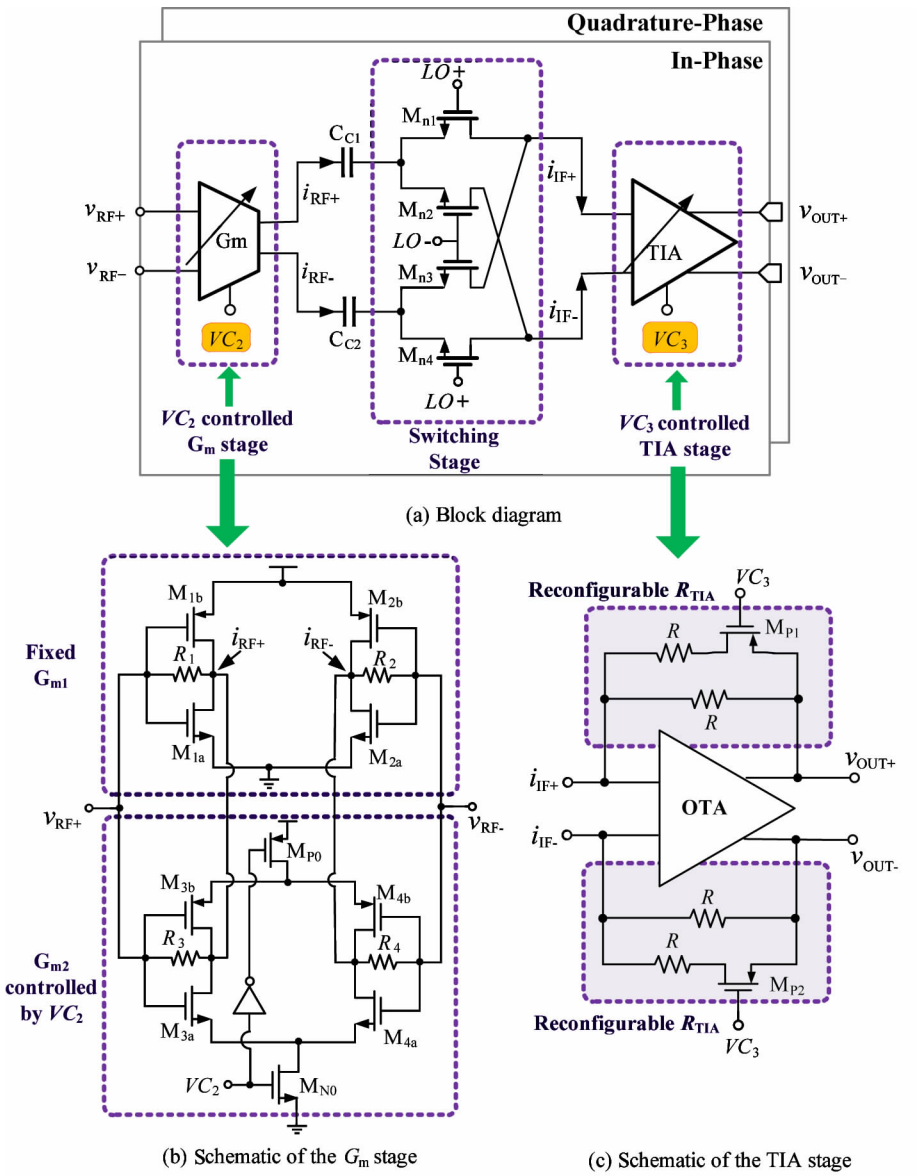

Fig. 5 Schematic of the proposed passive mixer

The TIA stage serves as the load, current to voltage converter and anti-aliasing filter for the mixer. The active-R TIA stage, as shown in Fig. 5(c), provides very low impedance at the switches output, so nearly all the signal current coming from the switches follows into the R_{TIA}. The reconfigurable R_{TIA} is a parallel combination resistor which is controlled by VC_3. When VC_3 is low, the effective transimpedance is $R/2$. On the contrary, it is R. Thus, the reconfigurable TIA provides another degree of freedom to configure the gain of the mixer.

In this work, the minimum VCG of mixer is set as

6 dB with a control word (0, 0). The 4 gain steps corresponding to a 2-bit control word ranges from 6 dB to 24 dB with a 6 dB step size according to the requirements of the selected communication standard. To fulfill the reconfiguration of *VCG*, the value of G_m and R_{TIA} is selected carefully. With the controllable G_m and R_{TIA}, the *VCG* can be set as 6, 12, 18, and 24 dB respectively as shown in Table 1.

Table 1 Reconfiguration of *VCG* versus the 2-bit control word

VC_2	VC_3	G_m(mS)	R_{TIA}(Ω)	*VCG*(dB)
1	1	12.8	2k	24
1	0	12.8	1k	18
0	1	3.2	2k	12
0	0	3.2	1k	6

A two stage miller compensated operational-transconductance amplifier (OTA) topology is chosen for the TIA design[8]. This structure can obtain both high output voltage swing and low input-referred noise. The cut-off frequency of the low pass filter is determined by the unit gain bandwidth of the OTA. In this work, in order to get a cut-off frequency of 15 MHz, the unit gain bandwidth of the OTA is needed to be as wide as 300 MHz.

The other critical block in the front-end is the local oscillator (LO) signal generation circuits. The required I and *Q* LO frequency ranges from 100 MHz to 3 GHz, while the divider operates between 0.2 GHz and 6 GHz. The divide-by-two was implemented in current-mode logic (CML) style which is depicted in Ref. [9]. The CML divider draws constant current and has the advantage of generating less current spikes during its dynamic operation. Because differential signaling is utilized in the CML divider, both I and Q LO outputs with good matching are available . Two scaled inverters are cascaded in each path to provide sufficient drive capability.

3 Measurement results

The wideband reconfigurable front-end is fabricated in TSMC 0.18 μm RF CMOS process. The die microphotograph is shown in Fig. 6 and whole chip occupies an area of approximately 1.17 mm^2 including pads.

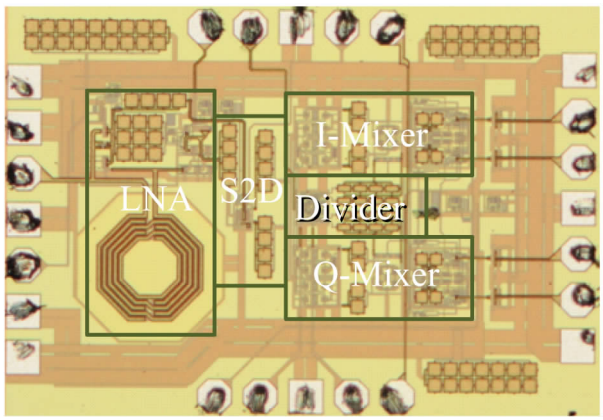

Fig. 6 Chip photograph of the wideband reconfigurable front-end

The reconfigurable front-end is required to handle wideband RF signals from 700 MHz to 2 600 MHz for compatibility with TD-LTE, FD-LTE, IoT, WCDMA, IEEE 802.11 b/g and other standards. The conversion gain and IF bandwidth are performed with the LO frequencies of 700 MHz and 2 600 MHz respectively. The conversion gain of the front-end has 8 steps around 18 dB to 39 dB, as shown in Fig. 7, by changing the control words (VC_1, VC_2, VC_3). The conversion gain only decreases 3 dB at f_{LO} = 2.6 GHz compared to 0.7 GHz. And the output bandwidth is larger than 14 MHz at any case which is suitable for all required wireless applications.

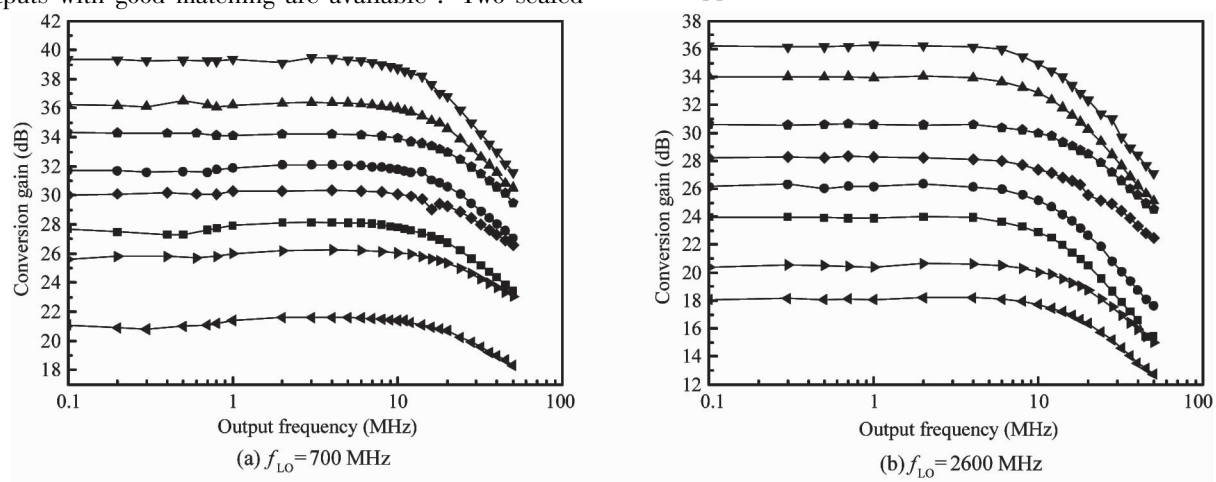

Fig. 7 Measured conversion gain of the proposed front-end with different f_{LO}

The front-end has the best linearity performance at the lowest gain. Two sinusoidal signals with frequencies of 705 and 705.5 MHz are applied to the input and f_{LO} = 700 MHz. The input power is swept from −30 dBm to −18 dBm with steps of 1 dB. Fig. 8 plots output power against input power for both linear output and third-order intermodulation components, giving an input third intercept point (IIP3) of −4.9 dBm.

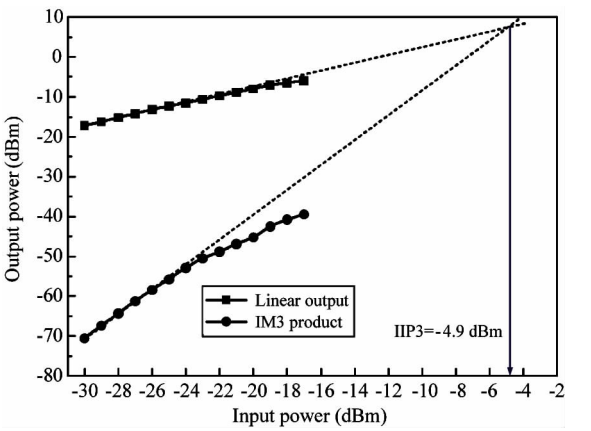

Fig. 8 Measured IIP3 of the front-end with f_{LO} = 700 MHz, f_{RF1} = 705 MHz, and f_{RF2} = 705.5 MHz at the lowest gain mode

The measured NF and power consumption of the front-end is shown in Fig. 9. The minimum NF of 4.6 dB is achieved at the highest gain mode, while the maximum NF of 9 dB is measured at the lowest gain mode. And the power consumption is 28 and 47.7 mW for the lowest and highest gain mode, respectively.

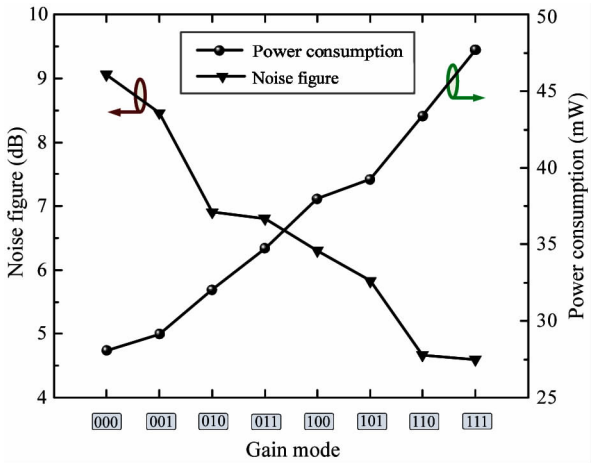

Fig. 9 Measured NF and power consumption under different gain mode at f_{LO} = 700 MHz

The measured results indicate that, by changing controlled words, the conversion gain of the front-end can be reconfigured according to the signal strength of the selected communication standard. Other characteristics such as NF, linearity can also be reconfigured consequently and the efficiency of power consumption can be enhanced greatly.

Table 2 summarizes the measured results of the proposed reconfigurable front-end and gives a comparison with other recently published wideband front-end. The comparison shows that the presented front-end achieves wide RF bandwidth along with competitive linearity, NF, and power consumption compared to other recently published work.

Table 2 Performance comparisons with resent publications

Specification	Ref. [10]	Ref. [11]	Ref. [12]	The proposed work
RF Input	Differential *	Single-ended	Differential *	Single-ended
Range (GHz)	0.6 – 3	0.048 – 0.86	0.5 – 2.5	0.1 – 2.9
Gain (dB)	42 – 48	40	5 – 17	18 – 39
Min. NF (dB)	3	5.5	3.7	4.6
Max. IIP3 (dBm)	−14	−10	0	−4.9
Power (mW)	30	140	12.3	28 – 47.7
Tech. CMOS	0.13 μm	0.18 μm	0.18 μm	0.18 μm

* Off-chip balun can result in an additional 1 – 1.2 dB NF degradation

4 Conclusions

This paper presents a single-ended wideband high dynamic range receiver front-end in 0.18 μm RF CMOS technology for MMMS applications. The reconfiguration strategies and design considerations are discussed. According to the selected operation mode, the switchable architecture minimizes power consumption while maintaining competitive performances for other parameters. Wafer measurement results indicate that the designed front-end can operate from 100 MHz to 2.9 GHz with good input match. The chip achieves voltage conversion gain from 18 dB to 39 dB with the minimum NF of 4.6 dB and the maximum IIP3 of −4.9 dBm. The IF bandwidth of the front-end is larger than 14 MHz

which can cover most of the standard's carrier frequencies. The characteristics of wideband, low noise, high linearity, moderate power and area consumptions make this implementation a good alternative in the applications of MMMS wireless communications.

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