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# Improved time-interleaved error feedback delta sigma modulator for digital transmitter application①

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**Abstract**

Time-interleaved structure can promote the equivalent processing speed of a digital signal processing system. An improved time-interleaved error feedback delta sigma modulator (TI-EF-DSM) for digital transmitter application is presented in this paper. Two TI-EF-DSMs are compared, one is a conventional directly implemented and the other is the improved. The processing speed of the proposed two-channel improved time-interleaved error feedback delta sigma modulator (ITI-EF-DSM) is higher than the conventional directly implemented TI-EF-DSM for shortened critical path. A digital transmitter based on the ITI-EF-DSM is implemented on field progrmmable gate array (FPGA). The long term evolution (LTE) signals with different bandwidths of 5 MHz, 10 MHz and 20 MHz are used as the signal source to evaluate the transmitter. The achieved SNR is 41 dB for the 20 MHz LTE signal with the processing clock of only 184 MHz.

**Key words**: time-interleaved, error feedback delta sigma modulator (EF-DSM), digital transmitter, long term evolution (LTE)

## 0 Introduction

High order modulation is used in modern wireless communication systems, such as QAM-64 and QAM256. They are usually used with orthogonal frequency division multiplexing (OFDM) for high spectrum efficiency. These signals are with non-constant envelop, and of high peak average power ratio (PAPR), so a linear power amplifier is required in the transmitter. To obtain lower distorted RF signals, a linear power amplifier (PA) in the RF transmitter often backs off severely. That leads to low drain efficiency of a power amplifier; and it shortens the working duration of battery supplied equipment. Many technologies have been developed to solve this contradiction. One of them is by using transmitter based on delta sigma modulator (DSM)[1-5].

DSM based transmitters need high sampling rate to suppress quantization noise generated by the delta sigma modulators. To process wideband signal, the clock frequency of a DSM needs several hundred megahertz or even more. In digital circuits, the clock speed is constrained by technology process. However, good designs can approach the available maximum clock speed as much as possible. Due to the short critical path and straightforward digital implementation, the error feedback delta sigma modulator (EF-DSM) is suitable for transmitter application. To promote the processing speed of the DSM, dedicated adders were designed[4]. Even higher processing speed can be realized by using time-interleaved structures[6-8].

Time-interleaved structure can be simply realized by polyphase decomposition[6,7]. The conventional time-interleaved structure from direct polyphase decomposition of an EF-DSM (called time-interleaved error feedback delta sigma modulator, TI-EF-DSM) suffers from long latency, which limits the maximum clock frequency. Adding appropriate pipelines in digital combinational logics in the critical path can promote the clock speed. By changing placement of the adder in the TI-EF-DSM, the path latency can be shortened.

This paper proposes a two-channel improved time-interleaved error feedback delta sigma modulator (ITI-EF-DSM). With the ITI-EF-DSM, the wideband signal, such as long term evolution (LTE) signal in 20 MHz mode can be processed with enough clock frequency, providing adequate signal to noise ratio (SNR). This

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paper is organized as follows. Section 1 gives the general structure of an EF-DSM based transmitter. A two-channel ITI-EF-DSM is described and simulated in Section 2. In Section 3, the ITI-EF-DSM based transmitter is built to enhance the bandwidth of the transmitter and FPGA validation is conducted. Finally, the conclusion is drawn in Section 4.

# 1 General structure of EF-DSM based transmitters

## 1.1 EF-DSM based transmitters

The block diagram of a general EF-DSM based transmitter is shown in Fig. 1. It is composed of four main parts[3-5]. The first is an EF-DSM to convert the baseband multi-bit signal into signal with several bits by using multi-bit quantizer. There are two identical EF-DSMs to process the input quadrature I/Q components respectively. The second is a digital frequency up-mixer to convert the signal into carrier frequency. The third is a high efficient switch mode power amplifier (SMPA) boosting the RF power to drive the antenna and the last part is a band-pass filter to remove the out-of-band quantization noise generated by EF-DSM.

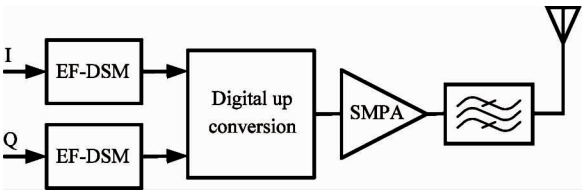



**Fig. 1** Block diagram of a general EF-DSM based transmitter

## 1.2 EF-DSMs

For a general EF-DSM, the relationship for the signal in Fig. 2(a) can be expressed as Eq. (1) and Eq. (2).

$$W(z) = X(z) + U(z) \tag{1}$$

$$Y(z) = V(z) + E(z) \tag{2}$$

The feedforward transfer function is unit, as Eq. (3).

$$H_{FF}(z) = 1 \tag{3}$$

The relationship of forward channel is

$$V(z) = H_{FF}(z)W(z) \tag{4}$$

The feedback transfer function is

$$H_{FB}(z) = 1 - (1 - z^{-1})^L \tag{5}$$

The relationship of feedback channel is

$$U(z) = -H_{FB}(z)E(z) \tag{6}$$

Considering the relationship for a quantizer:

$$Y(z) = V(z) + E(z) \tag{7}$$

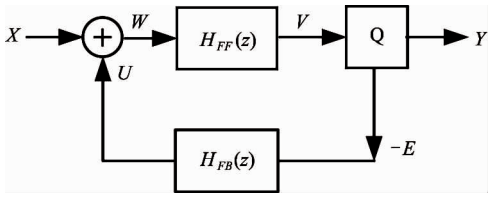
The transfer function of the EF-DSM can be expressed as

$$Y(z) = X(z) + NTF(z)E(z) \tag{8}$$

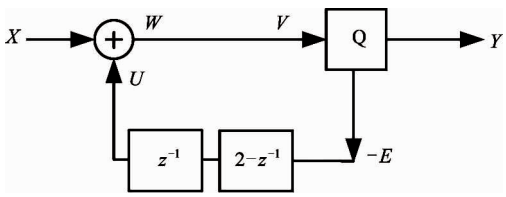
where,

$$NTF(z) = (1 - z^{-1})^L \tag{9}$$

A second order EF-DSM is realized as shown in Fig. 2(b) when $L = 2$.




(a) General EF-DSM




(b) Second order EF-DSM

**Fig. 2** EF-DSMs

# 2 Improved time-interleaved EF-DSM

## 2.1 General time-interleaved signal processing

In a general digital linear time invariant (LTI) signal processing system, the input and output relationship in $z$-domain is

$$Y(z) = H(z)X(z) \tag{10}$$

where, $X(z)$ and $Y(z)$ are $z$-transform of input and output sequence $x[n]$ and $y[n]$ respectively, and $H(z)$ is the transfer function of the LTI system. Its corresponding $M$-channel time-interleaved processing system is shown in Fig. 3 [6,7].

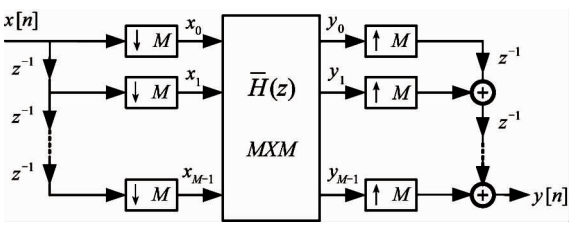



**Fig. 3** Diagram of time-interleaved signal processing

Serial input sequence $x[n]$ is delayed one by one with every $M$ sample in a group, generating a vector $\bar{\boldsymbol{x}}$.

$$\bar{\boldsymbol{x}} = (x_0 \quad x_1 \quad \cdots \quad x_{M-2} \quad x_{M-1})^{\mathrm{T}} \tag{11}$$

where, $x_0$ is newer than $x_{M-1}$. Then, signal $x[n]$ is processed in time-interleaved manners.

Processed by an appropriate parallel processing block $\bar{H}(z)$, another vector $\bar{\boldsymbol{y}}$ is generated.

$$\bar{\boldsymbol{y}} = (y_0 \quad y_1 \quad \cdots \quad y_{M-2} \quad y_{M-1})^{\mathrm{T}} \tag{12}$$

where, $y_0$ is newer than $y_{M-1}$.

With parallel-serial transform on $\bar{\boldsymbol{y}}$, the required output sequence $y[n]$ is generated.

The relationship of output $\bar{Y}(z)$ and input $\bar{X}(z)$ in $z$-domain for the parallel processing block $\bar{H}(z)$ is

$$\bar{Y}(z) = \bar{H}(z)\bar{X}(z) \tag{13}$$

where,

$$\bar{Y}(z) = [\,Y_0(z) \quad Y_1(z) \quad \cdots \quad Y_{M-2}(z) \quad Y_{M-1}(z)\,]^{\mathrm{T}} \tag{14}$$

$$\bar{X}(z) = [\,X_0(z) \quad X_1(z) \quad \cdots \quad X_{M-2}(z) \quad X_{M-1}(z)\,]^{\mathrm{T}} \tag{15}$$

$$\bar{H}(z) = \begin{bmatrix} E_0(z) & E_1(z) & E_2(z) & \cdots & E_{M-1}(z) \\ z^{-1}E_{M-1}(z) & E_0(z) & E_1(z) & \cdots & E_{M-2}(z) \\ z^{-1}E_{M-2}(z) & z^{-1}E_{M-1}(z) & E_0(z) & \cdots & E_{M-3}(z) \\ \vdots & \vdots & \vdots & \vdots & \vdots \\ z^{-1}E_1(z) & z^{-1}E_2(z) & z^{-1}E_3(z) & \cdots & E_0(z) \end{bmatrix} \tag{16}$$

where, $E_l(z)$ is the polyphase component of $H(z)$. If $e_l(n)$ is the time domain presentations of $E_l(z)$, the relation between $H(z)$ and $E_l(z)$ is as follows.

$$e_l[n] = h[nM - l] \quad 0 \leqslant l \leqslant M-1 \tag{17}$$

$$E_l(z) = \sum_{n=0}^{\infty} e_l[n]z^{-n} \tag{18}$$

and

$$H(z) = \sum_{l=0}^{M-1} z^{-l}E_l(z^M) \tag{19}$$

## 2.2 The TI-EF-DSM

According to Section 2.1, the polyphase decomposition elements for a two-channel TI-EF-DSM corresponding to Fig. 2(b) are as follows.

For the feed forward transfer function, it can be decomposed as

$$\begin{pmatrix} V_0 \\ V_1 \end{pmatrix} = \bar{H}_{FF}(z)\begin{pmatrix} W_0 \\ W_1 \end{pmatrix} \tag{20}$$

where,

$$\bar{H}_{FF}(z) = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \tag{21}$$

For the feedback transfer function, it can be decomposed as

$$\begin{pmatrix} U_0 \\ U_1 \end{pmatrix} = -\bar{H}_{FB}(z)\begin{pmatrix} E_0 \\ E_1 \end{pmatrix} \tag{22}$$

where, $E_0$ and $E_1$ are quantization noise for the two quantizers.

$$\bar{H}_{FB}(z) = \begin{bmatrix} -z^{-1} & 2 \\ 2z^{-1} & -z^{-1} \end{bmatrix} \tag{23}$$

The character of the quantizer is shown as Eq. (24).

$$\begin{pmatrix} Y_0 \\ Y_1 \end{pmatrix} = \begin{pmatrix} V_0 \\ V_1 \end{pmatrix} + \begin{pmatrix} E_0 \\ E_1 \end{pmatrix} \tag{24}$$

The relationship for the TI-EF-DSM can be expressed as Eq. (25).

$$\begin{pmatrix} Y_0 \\ Y_1 \end{pmatrix} = \begin{pmatrix} X_0 \\ X_1 \end{pmatrix} + \begin{bmatrix} z^{-1}+1 & -2 \\ -2z^{-1} & z^{-1}+1 \end{bmatrix}\begin{pmatrix} E_0 \\ E_1 \end{pmatrix} \tag{25}$$

The architecture for the two-channel TI-EF-DSM is shown in Fig. 4. There are two quantizers, three delays, and four adders in the TI-EF-DSM. The critical path is shown in dash line. It consists of four adders and two quantizers.

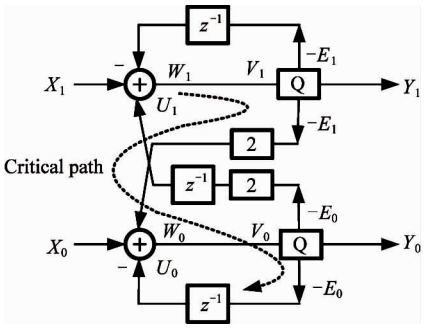
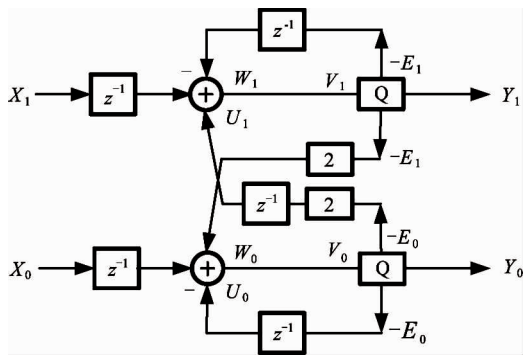


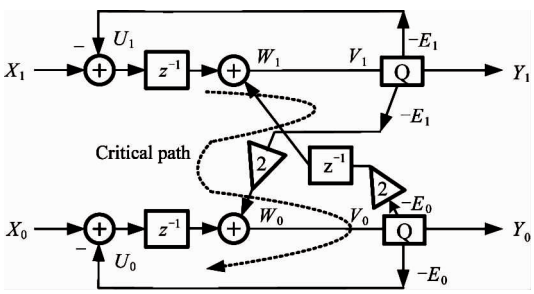

**Fig. 4** Direct implementation of the TI-EF-DSM

## 2.3 The ITI-EF-DSM

With additional two registers placed at the entrance of the TI-EF-DSM in Fig. 4, another TI-EF-DSM is got as shown in Fig. 5(a). With logic reduction, the proposed ITI-EF-DSM is obtained as shown in Fig. 5(b). The critical path in Fig. 5(b) is indicated




(a) The Improved time-interleaved EF-DSM with two additional delays




(b) The Improved time-interleaved EF-DSM with logic reduction

**Fig. 5** Improved time-interleaved EF-DSM

with dash line. It consists of three adders and two quantizers. Because the adders cause much delay in the TI-EF-DSM, so the critical path delay of ITI-EF-DSM is reduced. Therefore, the clock speed is promoted.

The transfer function in Fig. 5(b) can be expressed as

$$\begin{pmatrix} Y_0 \\ Y_1 \end{pmatrix} = \begin{pmatrix} z^{-1}X_0 \\ z^{-1}X_1 \end{pmatrix} + \begin{bmatrix} z^{-1}+1 & -2 \\ -2z^{-1} & z^{-1}+1 \end{bmatrix} \begin{pmatrix} E_0 \\ E_1 \end{pmatrix} \quad (26)$$

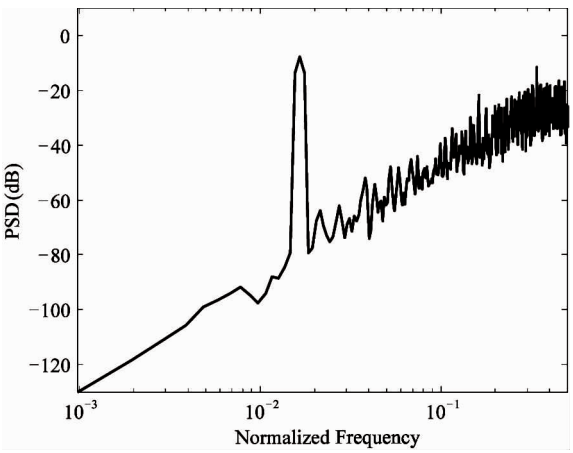
Considering the relationship of the two channels:

$$E_1 = z^{-0.5}E_0 \quad (27)$$

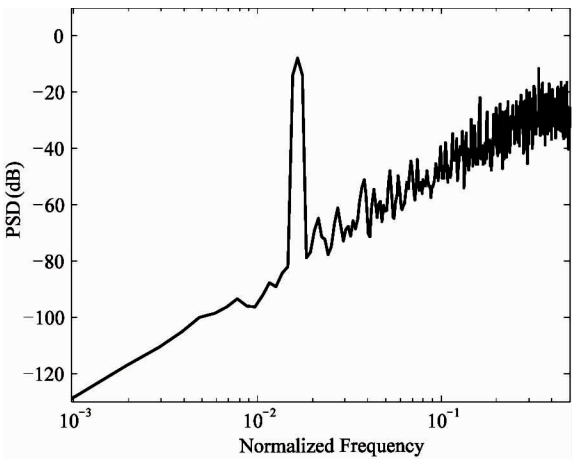
The equivalent single channel transfer function of the ITI-EF-DSM can be expressed as

$$Y(z) = z^{-2}X(z) + (1-z^{-1})^2E(z) \quad (28)$$

The noise transfer function is the same as Eq. (9). Although the signal transfer function in Eq. (28) is not unit, it is just two clock delays of the original signal $x$. To evaluate the correctness, the power spectrum density (PSD) simulation of the ITI-EF-DSM for single tone signal input is conducted using Matlab. Single tone full-scale signal with oversampling rate of 16 is used as the stimulus. PSD for TI-EF-DSM is also simulated with the same input signal for comparison. The normalized PSDs of the TI-EF-DSM and ITI-EF-DSM are shown in Fig. 6. The signals to noise ratios (SNRs) are 50.5 dB and 50.4 dB for the TI-EF-DSM and the ITI-EF-DSM respectively. They are almost the same. The simulation result confirms the correcness of the ITI-EF-DSM. TI-EF-DSM and ITI-EF-DSM are implemented on FPGA. Table 1 lists the synthesized results of three types of EF-DSMs. ITI-EF-DSM consumes largest hardware and gets the highest equivalent processing speed. Although TI-EF-DSM consumes less hardware, it gets lower maximum clock frequency. The non-time-interleaved EF-DSM consumes the least hardware, but the equivalent processing speed is the lowest.




(a) PSD of the two-channel TI-EF-DSM, SNR is 50.5 dB




(b) PSD of the two-channel ITI-EF-DSM, SNR is 50.4 dB

**Fig. 6** PSD of the two-channel TI-EF-DSM and ITI-EF-DSM

Table 1 Complexity and maximum clock speed of the EF-DSMs on FPGA

| | DFFs | Combination logics | Maximum clock speed (MHz) | Equivalent processing speed (MHz) |
|---|---|---|---|---|
| TI-EF- DSM | 26 | 62 | 151 | 302 |
| ITI-EF- DSM | 41 | 57 | 187 | 374 |
| EF-DSM | 26 | 31 | 257 | 257 |

## 3 Implementation of the ITI-EF-DSM based transmitter and experimental results

Fig. 7 is the implemented ITI-EF-DSM based transmitter. The digital baseband LTE signal is generated by Matlab at sampling frequency of 30.72 MHz. The IQ signals are then interpolated by 12 times up to 368.64 MHz and decomposed into two phases respectively. The decomposed digital streams are then imported into FPGA board as the signal source for the proposed transmitter. Two ITI-EF-DSMs implemented on

field programmable gate array (FPGA) are used to process the quadrature signals. A following multi-bit digital up converter transfers the signal center frequency into radio frequency in digital form, which is stored on the board. The stored RF signals are exported into PC for analysis.

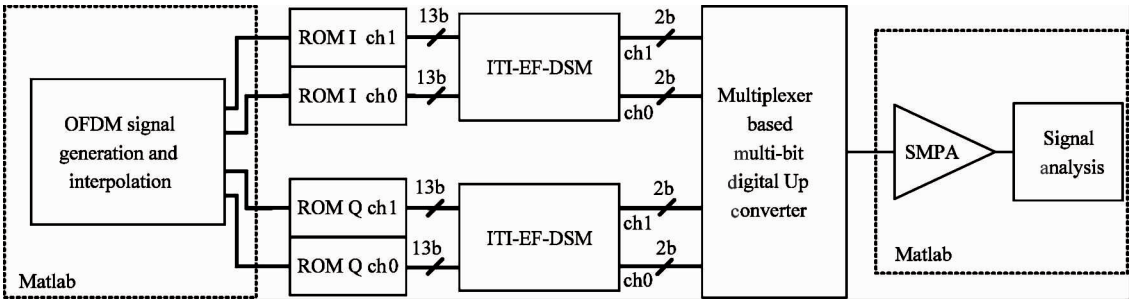



**Fig. 7** FPGA implemented ITI-EF-DSM based transmitter

### 3.1 Implementation of the digital up converter for ITI-EF-DSM based transmitter

The architecture for digital up converter is shown in Fig. 8. To implement the multiplexer based multi-bit mixer[3], a coding conversion unit is used before the up-conversion operation. For quantizer using mid-rise characteristic[9], output from the DSM could be signed odd values like $\{\pm 1, \pm 3\}$. The implemented EF-DSMs output sequences coding in two-bit signed format are converted into two-bit symmetric binary numbers before bit-wise digital up conversion. In the symmetric binary number, bit '0' presents positive, while bit '1' presents negative. The symmetric binary number for the two-bit signed number of output of the EF-DSM $\{-3, -1, 1, 3\}$ can be converted as $\{11, 10, 01, 00\}$. After coding conversion is the multiplexer based digital up converter. In Fig. 8, taking the most significant bit (MSB) of the symmetric binary number for example, the MSBs from the two channels are multiplexed into RF stream for MSB. In time-interleaving structure channel 0 is newer than channel 1, so, channel 1 should be processed in priority, and then is channel 0. Consequently, a sequence like $\{I_{MSB1}, Q_{MSB1}, \bar{I}_{MSB1}, \bar{Q}_{MSB1}, I_{MSB0}, Q_{MSB0}, \bar{I}_{MSB0}, \bar{Q}_{MSB0}\}$ is multiplexed out forming the digital RF sequence for MSB. The least significant bit (LSB) is processed with the same method.

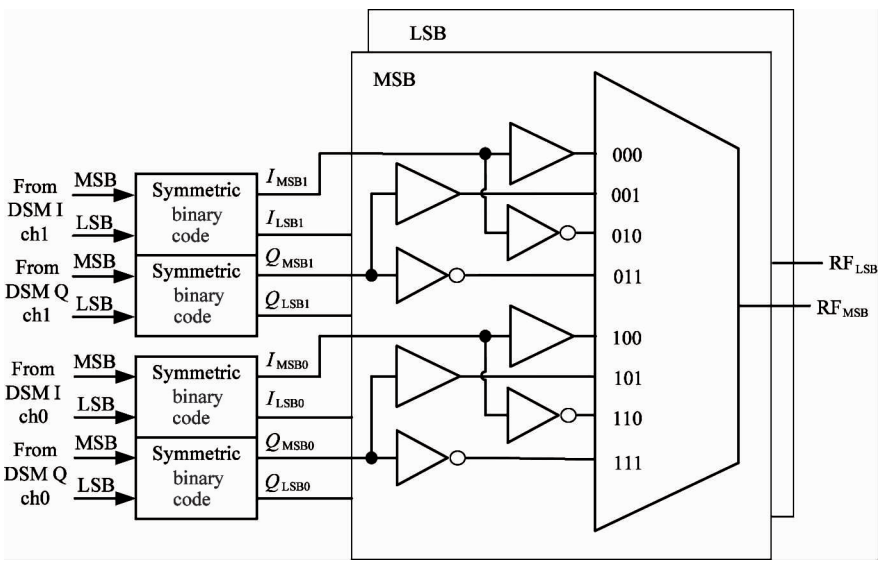
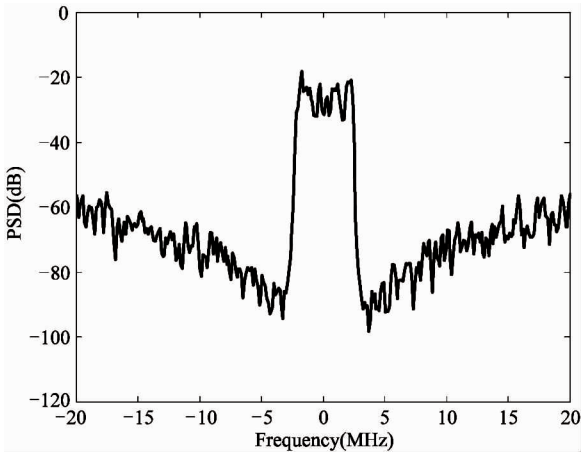



**Fig. 8** Multi-bit digital up converter for the transmitter

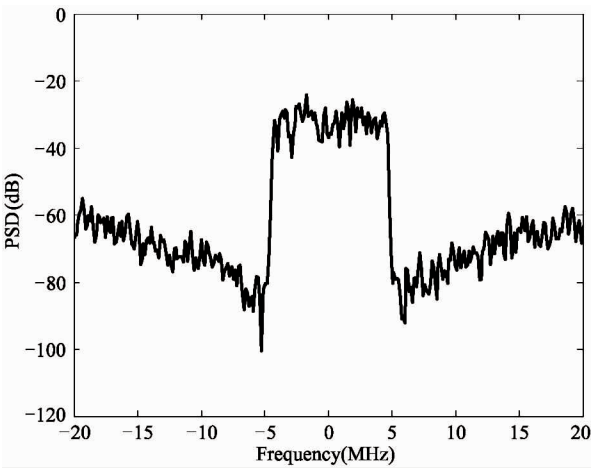
### 3.2 Experimental results

The LTE based OFDM signal with 5 MHz, 10 MHz and 20 MHz bandwidth are selected as the signal source to evaluate the proposed transmitter respectively. The two channel ITI-EF-DSMs run at clock of 184.32 MHz, and the equivalent processing speed is 368.64 MHz. The spectra results are shown in Fig. 9. Fig. 9(a) shows the signal bandwidth of 5 MHz. The

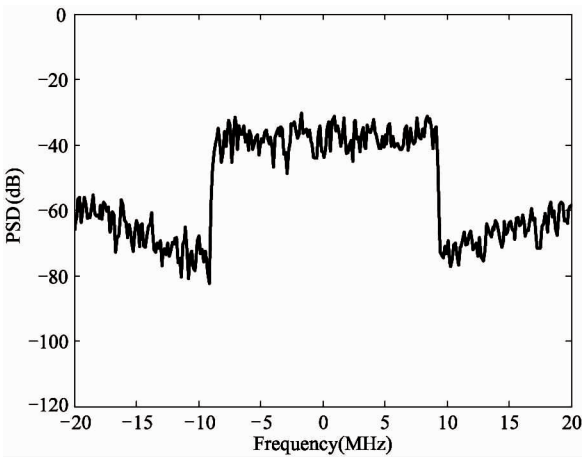
oversampling ratio (OSR) is 72 with the clock speed of 184.32 MHz; and the SNR is 70 dB. Fig. 9(b) shows the signal bandwidth of 10 MHz. OSR is 36 with the clock speed of 184.32 MHz; and SNR is 56 dB. Fig. 9(c) shows the signal bandwidth of 20 MHz. OSR is 18 with the clock speed of 184.32 MHz; and SNR is 41 dB. The clock speed for TI-EF-DSM should decrease to 150 MHz; and OSR for 20 MHz LTE signal is 15. The SNR for the TI-EF-DSM is 37 dB theoretically.




(a) PSD of 5 MHz LTE signal, SNR is 70 dB




(b) PSD of 10 MHz LTE signal, SNR is 56 dB




(c) PSD of 20 M LTE signal, SNR is 41 dB

**Fig. 9** PSDs for LTE signals

## 4 Conclusion

This paper proposes an improved time-interleaved error feedback delta sigma modulator for digital transmitter application. With the improvement, the clock speed of the modulator can be promoted. In the FPGA implemented ITI-EF-DSM based transmitter, the input LTE signal with bandwidth of 20 MHz is processed at the clock frequency of 184 MHz. And the output SNR of the transmitter achieves 41 dB. ITI-EF-DSM is valuable for delta sigma modulator based transmitters.

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