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Modeling and nonlinear analysis of 14 bit 100MS/s pipelined ADC①

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Abstract

In this paper, detailed models of 14-bit 100MS/s pipelined analog-to-digital converter (ADC) are presented. In order to help design of ADC system, blocks for pipelined ADC and disturbance sources are carefully analyzed. Critical parameters, such as capacitor mismatch, clock jitter are proposed and simulated. The pipelined ADC system is divided into five parts, clock generator, sample and hold (S/H) circuit, multiplying digital-to-analog converters (MDAC), backend, and digital correction. These blocks introduce several interferences, which attenuate performance of pipelined ADC severely. Modeling and simulations of these disturbance sources are presented particularly. A new model of S/H is introduced. Results derived from simulations can supervise design and optimization of the ADC system.

Key words: capacitor mismatch, offset, clock jitter, flip-around sample and hold (S/H), second-order response

0 Introduction

With great progress of analog-to-digital converter (ADC) technology, high-speed and high-precision ADC is the critical block in many applications, such as phased array radar[1,2]. Considering the complexity of the high-speed and high-precision ADC system, various disturbance sources, such as nonlinearity, noise and capacitor mismatch are introduced into the system, which decrease system performance seriously. In this situation, functional models of full ADC are absolutely necessary to evaluate impacts of different interferences. It is helpful to design circuit and simplify the design process.

Pipelined ADC could be divided into five blocks, i.e., sample and hold (S/H) circuit, MDACs, clock generator and backend, together with digital correction. In traditional way, these five blocks are usually described as simple ideal blocks, attached with some interferences source attached to system. However, in order to evaluate effects of disturbances and design ADC efficiently, this work focuses on modeling the blocks in mathematic way, with several key parameters selected from each block. It is helpful to analyze these parameters seriatim for circuit design and system optimization.

In traditional way, S/H circuit is often abstracted as a zero-order holding block, with offset block which stands for static gain error of operational amplifier (op-amp)[3]. This kind of modeling neglects complex circuit characters of op-amp, which is important in S/H block. In this work, a new model of S/H is proposed. The second-order linear system, together with slewing, is applied to modeling op-amp, which improves simulation accuracy. Besides, all these parameters, proposed in S/H model, could be obtained in g_m/i_d method[4,5], which do benefit S/H design a lot.

In pipelined ADC, clock jitter and thermal noise of op-amp are critical disturbance sources in the ADC system. They drastically aggravate the signal-to-noise ratio (SNR) of ADC. The parameters for these two models are vital in system design.

Also, output bits of each MDAC directly relate to complexity of circuit and power consumption of full ADC. Considering power consumption and performance of op-amp in MDAC, output bit of MDAC, which should be larger than 1.5bit, is a reasonable choice. However, the higher precision MDAC exports, the smaller reference voltage interval in MDAC is. In this situation, great pressure is posed on comparator design, which limits that output bits of MDAC could not be much higher. Instead of 1.5bit MDAC per stage——the traditional system arrangement, 2.5bit or 3.5bit MDAC is more often applied in MDAC design. As reference voltage interval deceases, offset from

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comparator affects system performance badly. In this case, power efficiency and system performance are both indispensable. Thus, trade off for MDAC design is necessary. In order to assist system design, simulation for MDAC is made carefully.

What's more, for pipelined ADC with high resolution, capacitor mismatch deteriorates system performance drastically. Based on the structure characters of pipelined ADC, effects of capacitor mismatching mainly lie on the first MDAC[6,7]. It is an important part to deal with in simulation.

1 Functional modeling of pipeline ADC

Pipelined ADC could be divided into five blocks. As described in Fig. 1, S/H circuit places at the front of ADC, followed by several MDACs with N bits digital output, and M bits flash ADC is at the end as backend. The N bits outputs from MDACs, together with M bits from backend are added up in digital correction, which generates 14 bit output of ADC. All the control signals are supplied by clock generator.

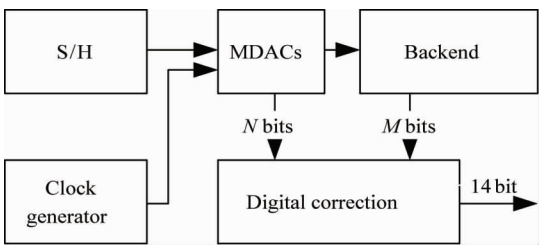

Fig. 1 Block of 14bit 100MS/s pipeline ADC

1.1 Sample and hold block

S/H circuit is critical in the ADC system, which ensures stability of S/H output in holding phase and decreases the effect of aperture uncertainty. Considering power limitation and complexity of circuit topology, flip-around S/H is the best choice. Fig. 2 is the structure of flip-around S/H circuit[8].

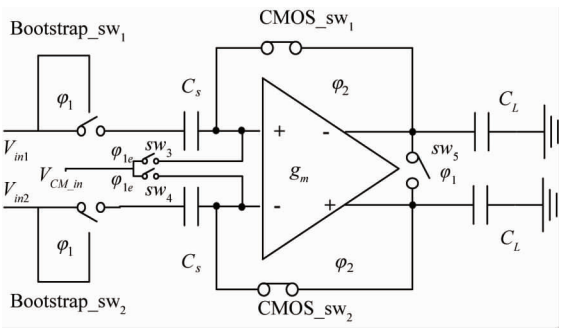

Fig. 2 Flip-around S/H

S/H circuit consists of op-amp and switch capacitors. Op-amp, a system with multiple zeros and poles, is the key circuit in S/H, whose performances are mainly related to its structure. Several structures, such as two stages and folded-telescope, are usually applied for op-amp design. Because folded-telescope op-amp is more power efficient, it is usually applied in S/H. Its structure is presented in Fig. 3[8,9].

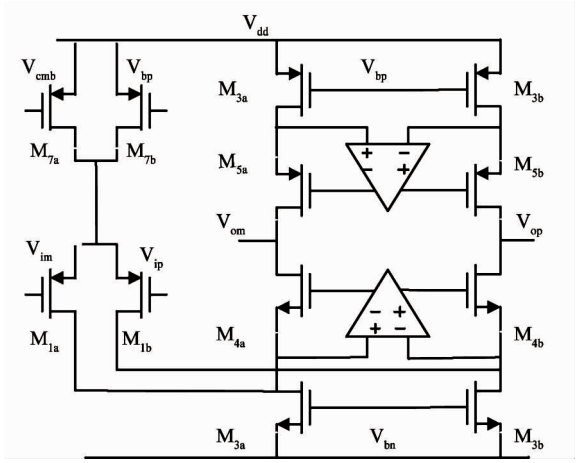

Fig. 3 Structure of folded-telescope op-amp

Because S/H is alternated in two phases, sampling phase and holding phase, the difficulty of modeling S/H mainly lies in dealing with the holding phase, in which op-amp works as negative-feedback. If input signal amplitude is large enough, the output response can be roughly divided into two parts, i. e. slewing and linear settling after slewing, in which slewing is capacitor charging process, which is proportional to charge current. And linear settling is process of linear system response.

In traditional way, for simplification, at the expense of reducing modeling precision, op-amp in S/H is usually modeled as a single pole system. On the contrary, more specific model is introduced.

In holding phase, for the one order system, when linear settling begins, derivative of response could be equal to slewing rate (SR), as shown in Eq. (1). It is continuous differentiable at the breaking point $V(t_{\text{slew}})$, which is critical in math. The one-order system response can be expressed as

$$\begin{aligned} V_1 &= SR \times t,\ t < t_{\text{slew}} \\ V_2 &= V_{\text{slew}} + (V_{\text{final}} - V_{\text{slew}}) \times (1 - e^{-\frac{t-t_{\text{slew}}}{\tau}}),\ t > t_{\text{slew}} \\ V_1(t_{\text{slew}})' &= V_2(t_{\text{slew}})',\ t = t_{\text{slew}} \end{aligned} \tag{1}$$

On the contrary, the model of S/H, applied in this paper, is a multiple poles system according to circuit analysis. When a large differential signal imports

to unit negative feedback system, capacitors of loading are charged. Compared to first-order system, output voltage charges to some extent, shown in Eq. (2), multiple poles response begins.

$$| V_{od} | = | V_{id} | \leqslant \sqrt{2} V_{vov} \mid v_{id} = 0 \tag{2}$$

As analyzed above, first-order system is too simple to evaluate the performance of op-amp. Two poles system is chosen to improve simulation accuracy, mainly depending on the circuit features that third pole and zeros of folded-telescope op-amp are far apart from the dominant and second pole. The second-order system for folded-telescope op-amp is shown in Eq. (3)[10,11].

$$\begin{aligned} a(s) &= a_0/(1 + s/\omega_1)(1 + s/\omega_2) \\ w_c &= a_0 \times \omega_1 \quad pm = \arctan \frac{\omega_2}{\omega_c} \end{aligned} \tag{3}$$

where, ω_1 is dominant pole, ω_2 is second pole, and a_0 is gain of op-amp. Thus, unit gain bandwidth ω_c, phase margin pm and static gain a_0 are key parameters, which could assist op-amp design.

In holding phase, the second-order system is connected as unit-negative feedback loop. In addition, derivative of linear system response is zero at the beginning of response settling. Thus, mathematically, the slewing and linear settling could not be continuously differentiable. Compared to the first-order system mentioned in Eq. (1), piecewise function is introduced here.

When loading capacitors are charged, voltage rises straight up in proportion of SR. Till input transistors operate in saturated state, linear setting begins. Because signal response is a continuous process, system response transfers from slewing to linear setting gradually. The piecewise function, a trade-off function applied for S/H modeling, extends response time, which offers some design margin. The model of S/H is presented in Eq. (4).

In Eq. (4), SR is slewing rate, V_{vov} is overdrive voltage of input transistor, a_0 is gain of op-amp, ω_1 is dominant pole, and ω_2 is second pole. These five variables are key parameters to evaluate performance of S/H[12,13].

As Eq. (4) shows, total response time could be divided into two parts, slewing time $t_{slewing}$ and linear setting time t_{lin}. $t_{slewing}$ is proportional to SR, which is determined by current of op-amp and loading capacitors. t_{lin} is related to gain of op-amp a_0, phase margin of negative feedback system, and gain band width product (GBW).

Simulation of these key parameters is presented in Section 2.

$$\begin{aligned} &\text{if} \quad V_i \leqslant \sqrt{2} \\ &V_{vov} \quad V_{out} = \sqrt{2} V_{vov} \times U(t) \otimes L\{A(s)\}^{-1} \\ &\text{if} \quad V_i > \sqrt{2} V_{vov} \\ &V_{out} = SR \times t, \ t \leqslant t_{slew} \\ &V_{out} = \sqrt{2} V_{vov} \times U(t - t_{slew}) \otimes L\{A(s)\}^{-1}, \ t > t_{slew} \\ &V_{slew} = V_{in} - \sqrt{2} V_{vov}, \ t = t_{slew} \\ &a(s) = a_0/(1 + \frac{s}{\omega_1})(1 + \frac{s}{\omega_2}), \ A_0 = a_0/1 + a_0 \\ &k = \frac{\omega_1 + \omega_2}{\omega_1 \omega_2}, \ w_0 = [\omega_1 \omega_2 (1 + a_0)]^{1/2} \end{aligned} \tag{4}$$

1.2 Clock jitter

Clock jitter is the critical disturbance in ADC system, which introduces harmonics, spurs in frequency spectrum and also raises noise floor. Effect of clock jitter is getting detrimental with rising of sample frequency and the jitter coupling from clock path to analog path also deteriorates the signal-to-noise-ration (SNR) of system.

Clock jitter is generally defined as

$$\begin{aligned} x(t + \delta) - x(t) &\approx 2\pi f_{in} \delta A \cos(2\pi f_{in} t) \\ &= \delta \frac{\mathrm{d}}{\mathrm{d}t} x(t) \end{aligned} \tag{5}$$

where, $x(t)$ is sinusoidal signal with amplitude A and frequency f_{in}, δ is infinitesimal.

Considering jitter as noise, it obeys Gauss distribution. Thus, noise power could be drawn up from Eq. (6)[14]:

$$\begin{aligned} E\{(x(t + \delta) - x(t))^2\} &= E\left\{ (\frac{\mathrm{d}x(t)}{\mathrm{d}t})^2 \delta^2 \right\} \\ &= E\left\{ (\frac{\mathrm{d}x(t)}{\mathrm{d}t})^2 \right\} E\{\delta^2\} \\ &= E\left\{ \left(\frac{\mathrm{d}}{\mathrm{d}t} A \cos(2\pi f_{in} t) \right)^2 \right\} \times \sigma_t^2 \\ &\cong (2\pi A_{RMS} f_{in})^2 \times \sigma_t^2 \end{aligned} \tag{6}$$

In Eq. (6), A_{RMS} is the RMS amplitude of the input signal with frequency f_{in}, σ_t is variance of noise sequence.

The noise power of jitter could be expressed as

$$N_{jitter} = (2\pi f_{in} A_{RMS} \sigma_t)^2 \tag{7}$$

In the model, σ_t, the variance of Gauss random signal, indicates the power of Gauss random signal. The random number block in jitter model produces Gauss random sequence with zero mean, and variance for σ_t^2. The simulation results and analyses are presented in Section 2.

1.3 Noise analysis of S/H circuit

According to the function of S/H, noise of S/H

circuit, a critical disturbance source, could be divided into two parts: noise in sampling phase and noise of op-amp in holding phase as shown in

$$\overline{V_{o.\,tot}^2} = \overline{V_{o.\,sam}^2} + \overline{V_{o.\,hold}^2} \tag{8}$$

When S/H works in sampling mode, noise power is mainly determined by sampling capacitor:

$$\overline{V_{o.\,sam}^2} = 2\frac{k.\,T_{emp}}{C_s} \tag{9}$$

It is generated by charging current accumulated on sampling capacitors. In this case, the integral noise will be transferred to the loading capacitor in holding phase.

When S/H works in holding phase, thermal noise of op-amp will be stored in loading capacitor. Because thermal noise is directly determined by circuit structure of op-amp, circuit of op-amp should be analyzed specifically.

As mentioned above, noise analyses for folded-telescope op-amp is necessary. In holding phase, half simplified circuit of folded telescope op-amp is shown in Fig. 4.

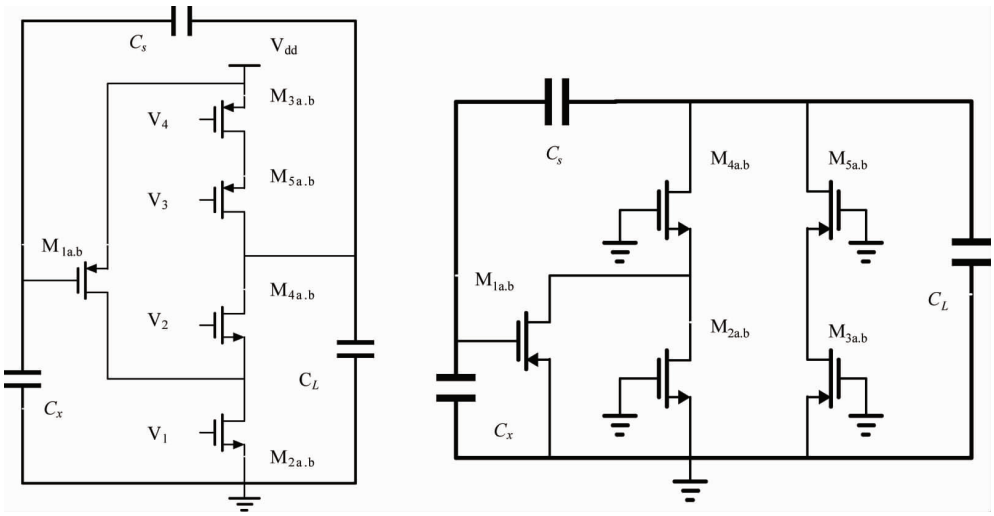

Fig. 4 Simplified circuit of folded-telescope op-amp

Its simplified noise model of small signal is shown in Fig. 5. Applying KCL and KVL, the noise could be concluded as

$$V_{n.\,out} = \frac{i_{n.\,1} + i_{n.\,2} + i_{n.\,3}}{C_L s + g_{m1}\beta},\ \beta = \frac{C_s}{C_s + C_x} \tag{10}$$

$$\overline{V_{o.\,hold}^2} = 2\left(1 + \frac{g_{m2}}{g_{m1}} + \frac{g_{m3}}{g_{m1}}\right)\frac{\gamma}{\beta}\frac{k.\,T_{emp}}{C_L},$$

$$\overline{V_{o.\,tot}^2} = 2k.\,T_{emp}\left[\frac{1}{C_s} + \left(1 + \frac{g_{m2}}{g_{m1}} + \frac{g_{m3}}{g_{m1}}\right)\frac{\gamma}{\beta}\frac{1}{C_L}\right] \tag{11}$$

$$\sigma_{C_s} = \left(\frac{2k.\,T_{emp}}{C_s}\right)^{0.5},$$

$$\sigma_{C_L} = \left(\frac{2k.\,T_{emp}}{C_L}\left(1 + \frac{g_{m2}}{g_{m1}} + \frac{g_{m3}}{g_{m1}}\right)\frac{\gamma}{\beta}\right)^{0.5} \tag{12}$$

In order to model noise in S/H, zero mean Gauss random sequence is introduced, with σ_{Cs} and σ_{C_L} as variance. For both the noise sources are not correlated, they could be added together directly with input signal.

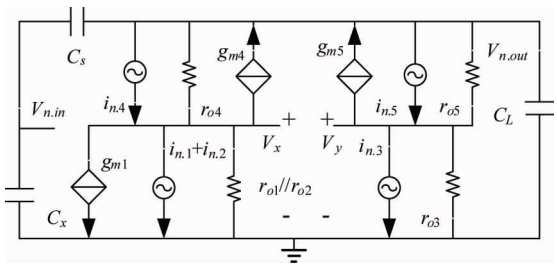

Fig. 5 Noise model of small signal

1.4 MDAC model

MDAC, the essential part of the whole ADC system, places behind S/H. Its structure is presented in Fig. 6.

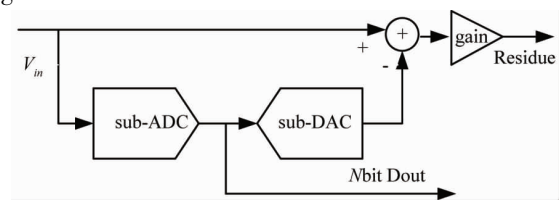

Fig. 6 Structure of MDAC

Because the op-amp in MDAC must meet the system requirements of MDAC, the more bits comparators in MDAC process, the less power op-amp consumes.

Considering traditional 1.5bit MDAC, it is less complex in structure, but power consumption booms up. Large gain and GBW of op-amp should be achieved, which both lead to large current consumption.

Compared to 1.5bit MDAC, 2.5bit MDAC is a better choice. Although, with the increase of output bits, power consumption of op-amp declines, the numbers of comparators applied in MDAC become almost double, which introduce several other problems, such as increase of MDAC complexity, and interval voltage of comparator reference decreasing. They all set barrier on the circuit design.

Similarly, 3.5bit MDAC shares the same merits with 2.5bit MDAC. However, pressure of meeting system demands is much greater than 2.5bit one. Since MDAC also introduces some interferences. The disturbances from MDAC could be divided into three parts: offset for comparator, gain error, and the error of sub-DAC (sDAC).

With the number of comparators increasing, attenuation of comparator offset would grow drastically. However, offset of comparator is not only contributed by the offset of comparator, it also contains the deviation of reference voltage. Moreover, as transistor scaling down and MDAC output bits increasing, the interval voltage for comparator reference deviates, which reduces the redundancy of offset voltage. Thus, the trade-off, between power consumption, output bits, and complexity of circuit design, is indispensable. In this work, simulation of offset for MDAC is presented.

In MDAC, capacitors mismatch is also a key disturbance source, which generates gain error and sDAC error. However, it is not the only source of sDAC error. In general, reference voltage deviation could also produce error in sDAC. In this study, capacitor mismatch and reference deviation are modeled and simulated separately.

1.5 Digital correction

Digital correction, aiming at rectifying the error introduced by comparator offset, is the critical algorithm for pipeline ADC[15].

Dislocation addictive is the core of digital correction algorithm. In order to overcome offset of comparators, the last bit of each stage is redundant bit. Digital correction is realized by full adder and clock alignment units. All the D_{out} of every stage are delayed by chronotron, in order to align with the clock. Then, through the full adder by dislocation addictive algorithm, 14bit output is achieved.

2 Simulations and analyses

Simulations have been performed for modeled blocks. The results are established below. Simulation of ADC with noise free is presented in Fig. 7. Because of noise free, only parameters of S/H are listed below:

Static gain (dB) = 108,

Unit gain bandwidth(GHz) = 1.2,

Phase margin (°) = 74.8

Considering the convergence time of simulation, all the performance of ADC is evaluated with 10MHz input. Capacitor mismatch is not introduced, same to reference voltage deviation, and the offset of comparator is null.

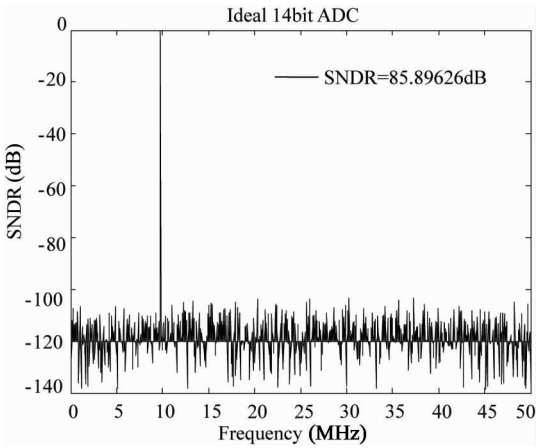

Fig. 7 4096 points FFT of 10MHz input without distortion

Fig. 7 shows 4096 points FFT of 14bit 100MS/s pipeline ADC with 10MHz input. As shown in Fig. 7, there is no harmonic distortion, the SNDR is 85.89626 dB, ENOB = 13.98277. The simulation result is close to theoretical analyses.

2.1 Simulation of S/H

The simulation of S/H aims at evaluating the performance of op-amp. Various parameters of op-amp, static gain, GBW, and phase margin, are combined together, which are simulated in groups.

As shown in Fig. 8 and Fig. 9, performance of ADC is diverse with changing of GBW. However, comparing Fig. 8 with Fig. 9, SNDR of ADC improves a little when gain increases. In other word, performance improving mainly depends on large GBW. As concluded above, gain does not play a critical role in S/H performance. Instead, GBW and phase margin are dominant factors.

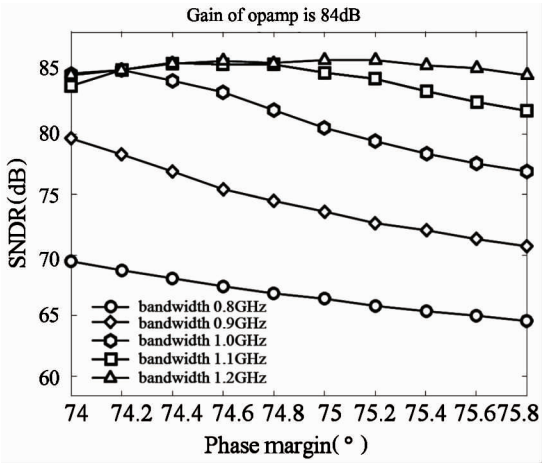

Fig. 8 SNDR of ADC with 84 dB op-amp in S/H

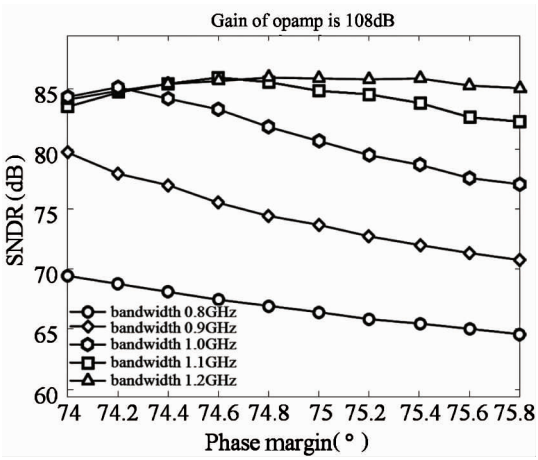

Fig. 9 SNDR of ADC with 108 dB op-amp in S/H

Referring to Fig. 10, Fig. 11, Fig. 12, and Fig. 13, 1.1GHz is a better choice for GBW. If the static gain meets performance requirement, with increasing of static gain, SNDR of ADC alters little. As results shown, phase margin of op-amp should be designed carefully within a reasonable range.

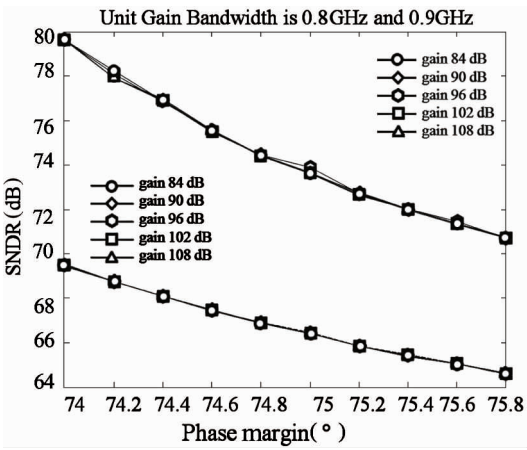

Fig. 10 SNDR with 0.8GHz and 0.9GHz GBW of op-amp

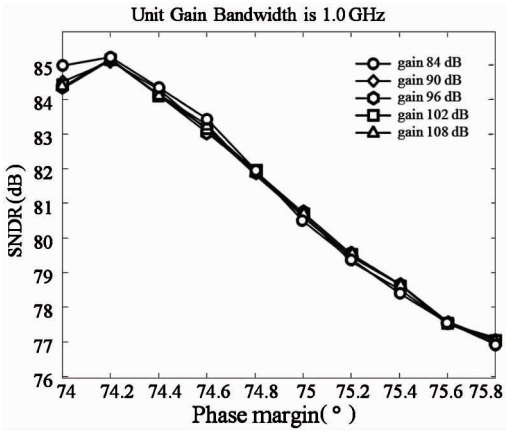

Fig. 11 SNDR with 1.0GHz GBW of op-amp

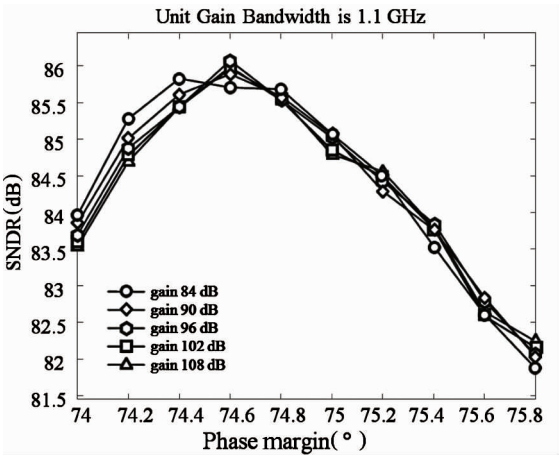

Fig. 12 SNDR with 1.1GHz GBW of op-amp

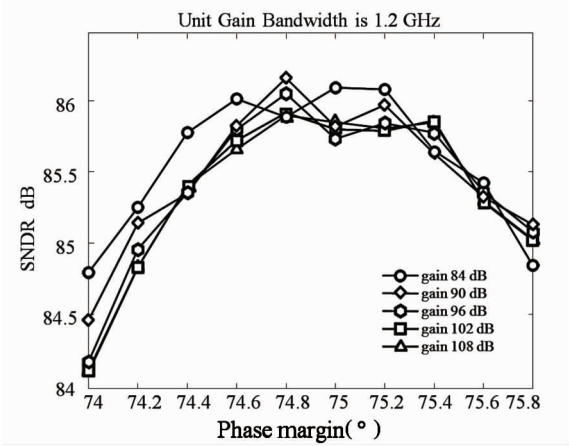

Fig. 13 SNDR with 1.2GHz GBW of op-amp

2.2 Simulation of clock jitter

For a 14bit ADC, noise free, SNR of system should be 86dB at least. The clock frequency is 100MHz, input signal amplitude is 1.5Vp-p.

The total noise of ADC could be described as

$$N_{tot} = N_{low\_fre} + N_{jitter} \quad (13)$$

Total SNR is given by

$$SNR_{\text{tot}} = 10\log[S/(N_{\text{low\_fre}} + N_{\text{jitter}})] \quad (14)$$

It can be concluded as

$$\sigma_t = \frac{\sqrt{N_{\text{jitter}}}}{2\pi f_{in} A_{\text{RMS}}} = \frac{\sqrt{\frac{S}{10^{\text{snrt}/10}} - \frac{S}{10^{\text{snr\_low\_fre}/10}}}}{2\pi f_{in} A_{\text{RMS}}}$$

$$= \frac{\sqrt{\frac{1}{10^{\text{snrt}/10}} - \frac{1}{10^{\text{snr\_low\_fre}/10}}}}{2\pi f_{in}} \quad (15)$$

For clock jitter simulation, if the ADC is abstracted as a noise-free system, and SNDR 86 dB, thus $\sigma_t \leqslant 0.1595$ps.

Fig. 14 illustrates the clock jitter effects on ADC system. As σ_t increasing, the performance of system severely deteriorates. Fig. 15 and Fig. 16 present ADC SNDR under specific clock jitter. Comparing Fig. 15 with Fig. 16, with σ_t increasing, the noise floor of ADC SNDR increases. Referring to math analysis above, the simulation results are in agreement with parameter estimation.

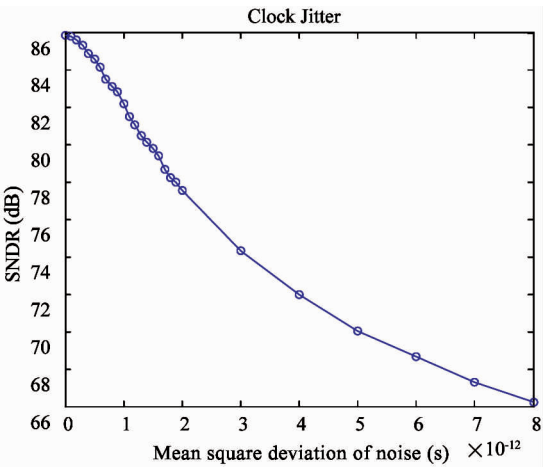

Fig. 14 Jitter impact on 14bit ADC with 10MHz input

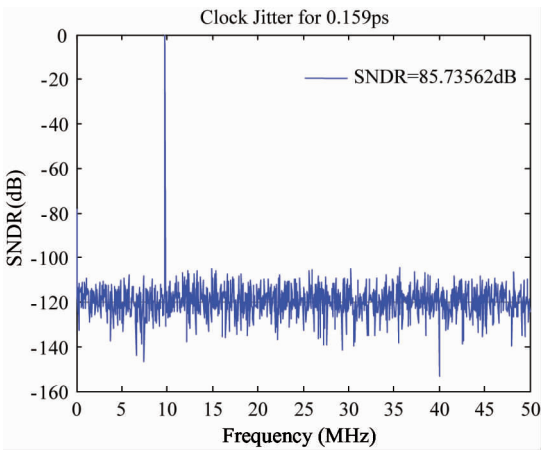

Fig. 15 SNDR of ADC with 0.159ps jitter

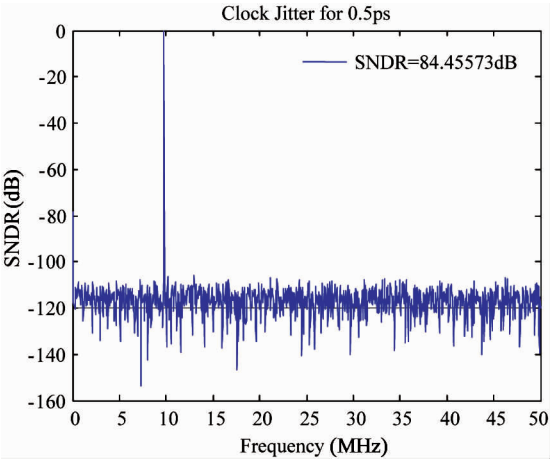

Fig. 16 SNDR of ADC with 0.5ps jitter

2.3 Simulation of S/H noise

Noise simulation in S/H is derived from the analysis of circuit structure. All the parameters could be abstracted by g_m/i_d methods. Based on this method, parameters iteration could improve simulation accuracy.

As described in Eq. (12), C_s, C_L and g_{m1} are key parameters in noise evaluation. Simulation refers to ratio of C_s to C_L. And a series of curves related to C_L are presented in Fig. 17.

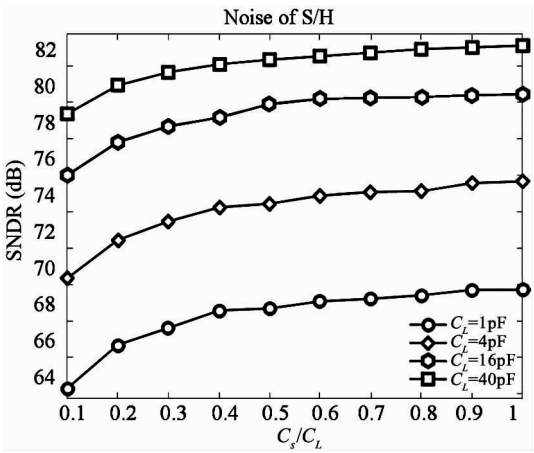

Fig. 17 Noise of S/H

Two SNDR results, compared in Fig. 18 and Fig. 19, illustrate that nearly 40pF for C_s and C_L obsess ENOB of 14bit. However, large capacitor directly relates to large power consumption, large chip area. 40pF capacitor for S/H design is almost impossible.

In this situation trade-off is necessary. Fig. 19 presents the simulation result of 4pF capacitor for C_s and C_L, which shares 75.66dB SNDR, nearly 13bit for ENOB. Considering system design, it is reasonable that kind of performance reduction exchanges for power efficient.

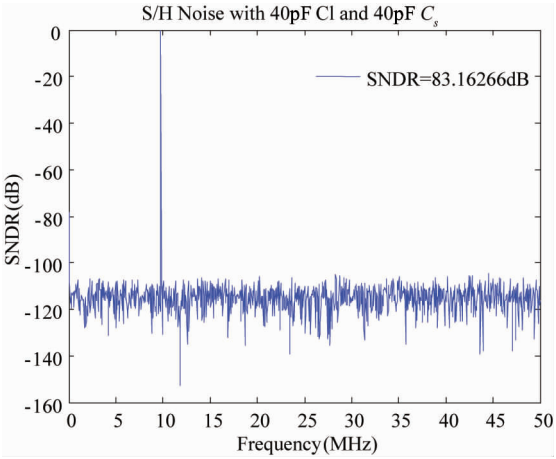

Fig. 18 SNDR of ADC with 40pF sample capacitors

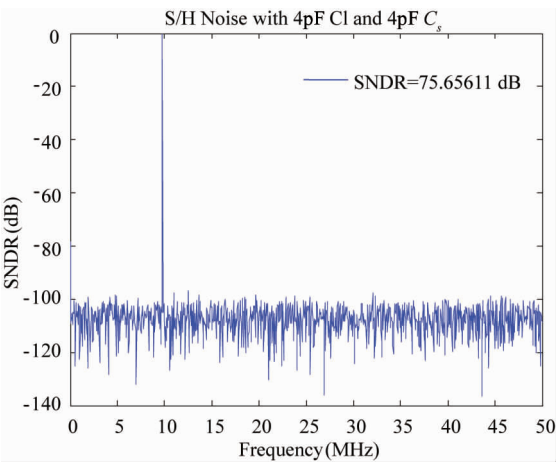

Fig. 19 SNDR of ADC with 4pF sample capacitors

2.4 Simulation of capacitor mismatch in MDAC

Capacitor mismatch in MDAC is another important disturbance source in ADC. Because 1st MDAC suffers from capacitor mismatch severely, simulations aim at 1.5bit MDAC, 2.5bit and 3.5bit MDAC separately.

The transmission formula of 1.5bit MDAC is

$$V_o = \begin{cases} (1+\dfrac{C_s+\Delta C_s}{C_f})V_i + \dfrac{C_s+\Delta C_s}{C_f}V_{\text{ref}}, & V_i > \dfrac{V_{\text{ref}}}{4} \\ (1+\dfrac{C_s+\Delta C_s}{C_f})V_i, & -\dfrac{V_{\text{ref}}}{4} \leqslant V_i \leqslant \dfrac{V_{\text{ref}}}{4} \\ (1+\dfrac{C_s+\Delta C_s}{C_f})V_i + \dfrac{C_s+\Delta C_s}{C_f}V_{\text{ref}}, & V_i < -\dfrac{V_{\text{ref}}}{4} \end{cases} \tag{16}$$

Though C_s should equals to C_f, water process introduces capacitors mismatch.

$$1+\frac{C_s+\Delta C_s}{C_f} = 2(1+\frac{1}{2}\sigma), \quad \frac{C_s+\Delta C_s}{C_f} = 1+\sigma \tag{17}$$

In Eq. (17), σ is capacitor deviation ratio, which is given in process manual. Capacitor deviation ratio is directly related to the area of square capacitor. As given in process manual, 0.15% deviation ratio corresponds to 20μm plus 20μm square capacitor, and 0.25% deviation ratio for 10μm plus 10μm square capacitor.

Fig. 20 presents simulation results of 0.25% capacitor mismatch for 1.5bit MDAC, and Fig. 21 is SNDR of capacitor deviation ratio 0.15%.

As shown in Fig. 20 and Fig. 21, it is obvious that performance degrades severely due to capacitor mismatch, which leads to severe harmonic distortion. With deviation ratio decreasing, performance improves a bit. However, it is still far beyond the requirement of 14bit ADC.

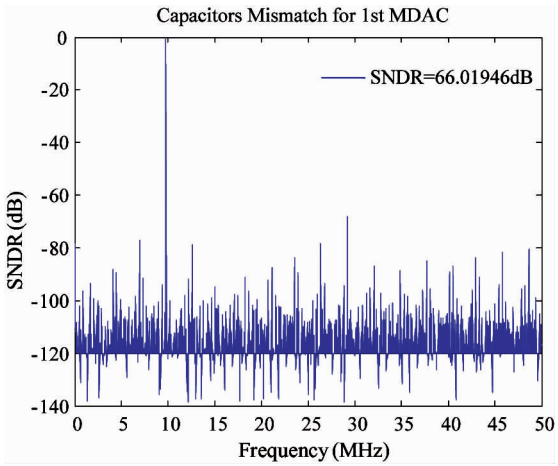

Fig. 20 0.25% capacitor mismatch for 1.5bit MDAC

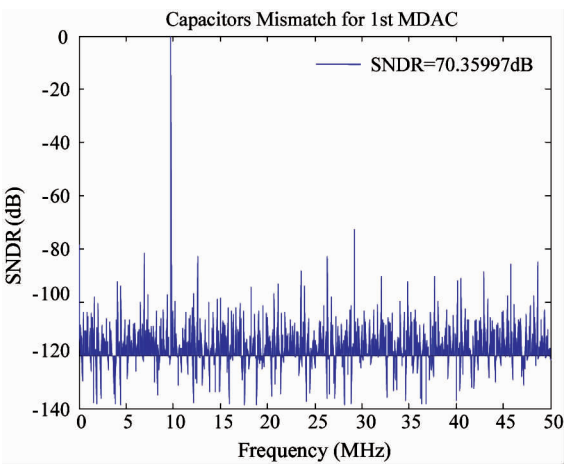

Fig. 21 0.15% capacitor mismatch for 1.5bit MDAC

The transmission formula of 2.5bit MDAC is similar to that of 1.5bit MDAC. Fig. 22 and Fig. 23 present simulation of capacitor mismatch for 2.5bit MDAC.

According to simulation results, SNDR of 2.5bit MDAC is better than that of 1.5bit one. It concludes that capacitor mismatch distortion in 2.5bit MDAC is

less than that in 1.5bit MDAC. However, odd harmonic distortions are still severe, which deteriorate the ADC performance drastically.

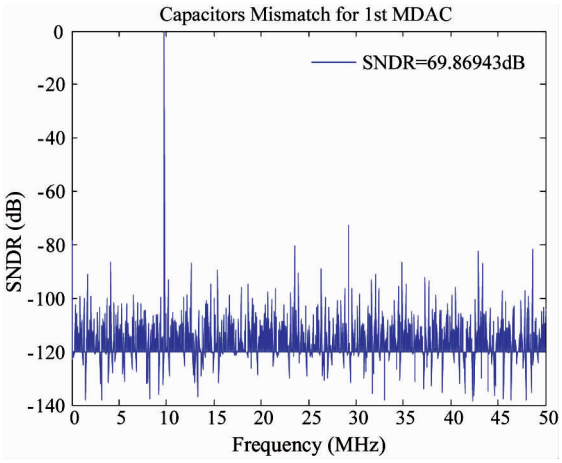

Fig. 22 0.25% capacitor mismatch for 2.5bit MDAC

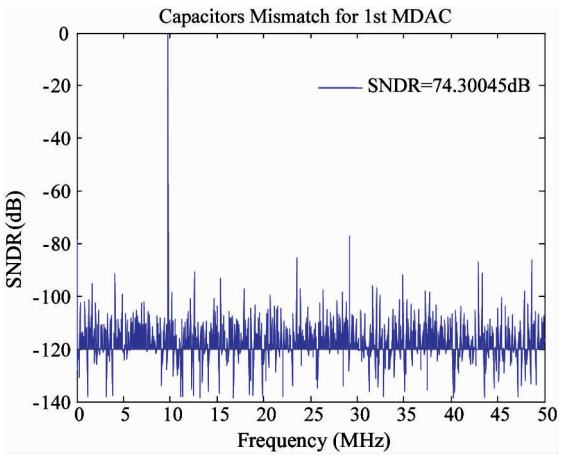

Fig. 23 0.15% capacitor mismatch for 2.5bit MDAC

Because 3.5bit MDAC shares the similar model with other MDACs above, its transmission formula is more complex, thus, only simulation results of 3.5bit MDAC is presented in Fig. 24 and Fig. 25.

From the simulation results above, shown in Fig. 24 and Fig. 25, it is evident that capacitor mismatch for 3.5bit MDAC affects less than that of 2.5bit MDAC, even less than that of 1.5bit one. However, a little bit improvement still could not fulfill the requirements of 14bit system.

Considering the system design, as the output accuracy of MDAC is higher, the effect of capacitors mismatch is lower. However, higher output accuracy of MDAC leads to great design pressure of comparator. In this situation, trade-off is necessary. A kind of digital calibration algorithm for capacitor mismatch should be applied in 14bit ADC.

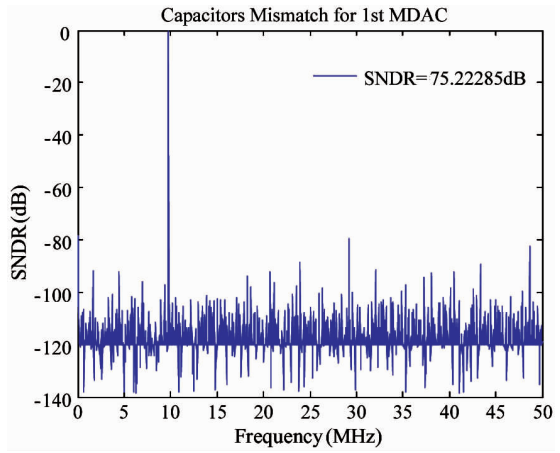

Fig. 24 0.25% capacitor mismatch for 3.5bit MDAC

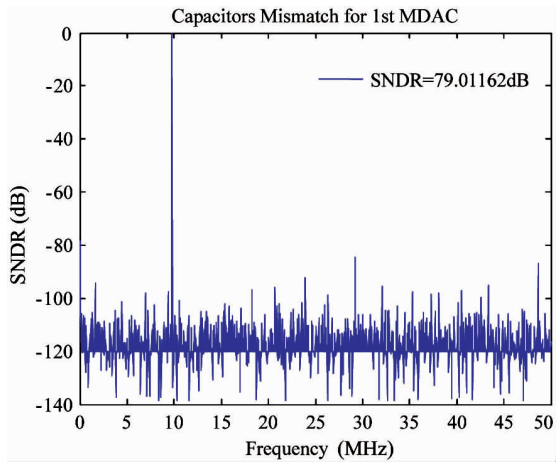

Fig. 25 0.15% capacitor mismatch for 3.5bit MDAC

2.5 Simulation of comparator offset in MDAC

As introduced in Section 2, digital correction could be applied to correct offset of comparator. If offset of comparator is over the range of digital correction, the performance would also be degraded.

Because negative half reference voltages are symmetric to the positive ones, only simulation of positive half is presented in Fig. 26.

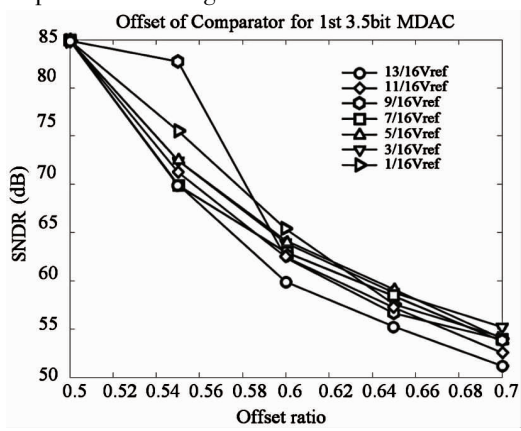

Fig. 26 Offset of comparator for 1st 3.5bit MDAC

Referring to Fig. 26, curves share the similar trend of performance degradation, and offset affects ADC SNDR badly. In this case, comparator circuit needs fabricating carefully.

2.6 Simulation of reference voltage deviation in MDAC

Although in ADC all the bias voltages are generated by the same band-gap, tiny disturbance to bias, such as noise, voltage loss on metal line, would degrade system performance. Because reference voltage deviation also generates distortion, it is important to take reference voltage deviation into consideration. Take 3.5bit MDAC as an example.

From SNDR curves shown in Fig. 27 above, it is obvious that 0.1% deviation of bias voltage causes great attenuation to the system. Bias circuit design and layout should be fabricated carefully

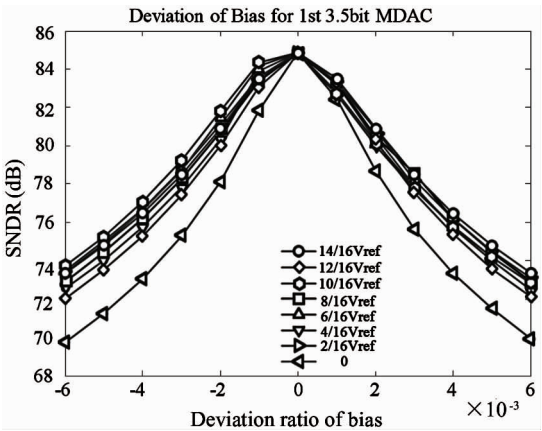

Fig. 27 Deviation of bias for 3.5bit MDAC

3 Conclusion

In this research, functional models are fabricated for 14bit 100MS/s pipelined ADC. Referred to the simulations and analyses in the paper, ADC could be abstracted as one import system with several disturbance sources, such as noise, bias deviation, jitter and capacitor mismatching, which are analyzed and modeled carefully in this paper. According to the analyses, several key parameters are proposed in this paper. All these parameters could be obtained from pre-design in g_m/i_d method. After pre-design in g_m/i_d method, parameter iteration could improve simulation accuracy. According to the simulation results, not only circuit design could be done carefully, but also layout of circuit would be fabricated precisely, such as square capacitor choosing, and bias voltage wiring.

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