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Design and validation of real-time dynamic spectrum management in OFDM-based HNPLC systems①

Liu Wenjing (刘雯静)*, Guo Jingbo②*, Yan Yanxin**, Zhang Tongfei*
(*State Key Lab of Control and Simulation of Power Systems and Generation Equipment, Department of Electrical Engineering, Tsinghua University, Beijing 100084, P. R. China)
(**ROHM Semiconductor (Shanghai) Co., Ltd. Design Center, Shanghai 200333, P. R. China)

Abstract

Time-varying frequency selective attenuation and colored noises are unfavorable characteristics of power line communication (PLC) channels of the low voltage networks. To overcome these disadvantages, a novel real-time dynamic spectrum management (DSM) algorithm in orthogonal frequency division multiplexing (OFDM)-based high-speed narrow-band power line communication (HNPLC) systems is proposed, and the corresponding FPGA circuit is designed and realized. Performance of the proposed DSM is validated with a large amount of network experiments under practical PLC circumstance. As the noise in each narrow subcarrier is approximately Gaussian, the proposed DSM adopts the BER/SER expression formulized via the AWGN channel to provide a handy and universal strategy for power allocation. The real-time requirement is guaranteed by choosing subcarriers in group and employing the same modulation scheme within each transmission. These measures are suitable for any modulation scheme no matter the system criterion is to maximize data rate or minimize power/BER. Algorithm design and hardware implementation of the proposed DSM are given with some flexible and efficient conversions. The DSM circuit is carried out with Xilinx KC705. Simulation and practical experiments validate that the proposed real-time DSM significantly improves system performance.

Key words: real-time dynamic spectrum management, high-speed narrowband power line communication (HNPLC), subcarrier grouping, rate adaptive, multi-carrier

0 Introduction

Paramount properties of modern power system are smart, reliable, green, and economical and compact, which stringently need a proper information-exchanging scheme embedded inside the power system to strengthen security and intelligence[1,2]. High-speed narrowband power line communication (HNPLC), providing a proper data rate of Kilo-bits per second via the inherent power line of the power system, is regarded as the preferred solution for both urban and long-distance rural applications for smart grid[3,4].

A lot of attentions, both in industrial and academic fields, have been paid to the development of HNPLC, for it provides a compact, intelligent and reliable method for information interaction of smart grid[5,6], such as advanced metering infrastructure (AMI), bidirectional transmission of local control signals in micro grids, charging and discharging management of electric vehicle (EV), et al. However, the HNPLC channel is far from ideal for high-quality communications due to its adverse time-varying frequency selective attenuation and colored noises[7,8]. In order to combat the deleterious environment, dynamic spectrum management (DSM) technology combining with orthogonal frequency division multiplexing (OFDM) is regarded as an excellent solution for enhancement of communication performance[9]. The DSM coordinates the available resources to meet required constraints as well as to adapt to the time-varying frequency selective attenuated and colored noisy channel. There are a lot of challenges to be overcome to implement DSM in a realistic HNPLC system.

DSM technology dynamically selects the available subcarriers and determines the best modulation scheme according to signal to noise ratio (SNR) of each subcarrier in multi-carrier systems[10] so as to obtain the

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② To whom correspondence should be addressed. E-mail: guojb@tsinghua.edu.cn
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maximal transmission rate or minimal bit error rate (BER) under the given power. Too much attention has been paid to various algorithms[11,12] in previous work, such as water-filling algorithm[13], Hughes-Hartogs[14,15], Chow[16] and Fischer algorithm[17], to name a few. Water-filling algorithm is easily understood, but the constellation size or transmitted bits obtained from the algorithm may not be an expected integer, in which the constellation can't be realized if the size is directly rounded to obtain the approximation. Hughes-Hartogs algorithm (also named as bit-loading algorithm) needs a mass of sorting and searching operations to get the optimal result, which is too complex to be applied in real-time power line communication systems. Chow algorithm sets equal power to each subcarrier to reduce the computational cost. However, the allocated bits under the power constraint are not optimal. Fisher algorithm gives the closed-form of bit and power allocation with relative low computational complexity, but it has constant data rate, which is contrary to the rate adaptive criteria[18]. Although the optimal DSM algorithm and its variants have been proposed and discussed widely, the design and realization of real-time DSM in PLC is found seldom and its performance in practical HNPLC environments has got little insight in previous literatures.

Actually it is important to realize that there are only limited resources for practical HNPLC systems to execute DSM, i.e. limited computing time and limited hardware resources. Especially in the time-varying frequency selective attenuated and colored noisy circumstance, a fast response of the adaptive scheme is needed urgently when electrical appliances are switched on or off in the network[19]. This paper aims to design a real-time DSM algorithm and execute it in the practical HNPLC system to validate its efficiency and reliability.

The uniqueness and key contributions of the proposed real-time DSM are three aspects:

(1) The proposed DSM provides a handy and universal method to use the formulated BER/SER expression for power allocation with no constraint on the modulation scheme. In most published work, the quadrature amplitude modulation (QAM) is employed in DSM algorithm for the OFDM based system[20,21], while DPSK-OFDM is generally adopted in HNPLC system, for example, in G3-PLC[22] and PRIME[23]. Based on the fact that the noise of each narrow subcarrier in HNPLC is approximately Gaussian, it is appropriate to take advantages of BER/SER expression formulated via the AWGN channel to guide resources allocation.

(2) To meet the real-time requirement, subcarrier grouping and same modulation scheme are employed in each transmission to reduce overhead cost and computational complexity in the proposed DSM. This way provides an applicable solution to real-time DSM for any rate-maximum or power/BER-minimum systems, and this paper takes a rate-maximum HNPLC system as a paradigm.

(3) Some flexible and efficient conversions are also elaborated in the design and its corresponding realization of hardware circuit for the proposed real-time DSM, as to facilitate any similar cases.

The organization of this paper is as follows. In Section 1, the HNPLC physical layer (PHY) profile is introduced and its related parameters to the real-time DSM are described. In Section 2, the mathematic design is developed and the proposed real-time DSM algorithm is efficiently realized. In Section 3 and Section 4, performance simulation and hardware implementation are carried out respectively. In Section 5, network experiments to validate the proposed DSM circuit with KC705 is presented. Finally conclusion is drawn in Section 6.

1 Profile of HNPLC physical layer

Implementation of DSM relies on the HNPLC specification of physical layer. Thus it is necessary to describe the PHY specification first. As most research work of this paper is obtained in China, specific circumstance of China is set up in the following description. However, the algorithm and system framework can also be applied to other narrowband power line communication system, such as FCC, ARIB and CENELEC A/B/C, by masking certain tones or transforming the related parameters.

1.1 PHY artchitecture

One of the main functions of the physical layer of a PLC transceiver is to construct a protocol frame to comfort data transmission via specific medium. There are commonly three parts in the HNPLC PHY frame, as shown in Fig. 1, which are preamble, frame control header (FCH) and data payload.

The preamble is constituted by several predefined symbols for package detection and SNR estimation to conduct DSM. FCH tells the obligatory information for demodulation whose length indicates the overhead cost of DSM. Besides the coding and interleaving techniques, similar with G3 PLC[24], data payload takes the real-time DSM for QoS guarantee. Overlapping and windowing are applied for inhibition of spectrum leakage.

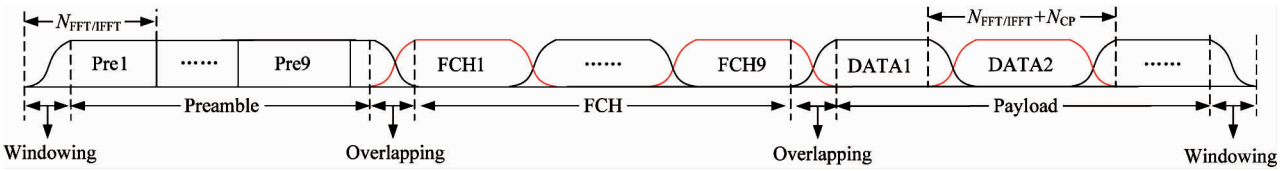

Fig. 1 Typical PHY frame structure of HNPLC system

1.2 Key parameters of physical layer

With consideration of related compulsory regulations and statistical transmission characterization of channel and noise in the HNPLC system[8,25,26], the key parameters of the PHY specification are listed in Table 1. Legal modulation schemes include DBPSK, DQPSK and D8PSK. ROBO modulates the data in DBPSK with 4-times repetition coding. The length of OFDM FFT/IFFT is 256 in which 96 subcarriers are defined for data transmission. The transmission frequency occupies 37.5kHz to 482.8125kHz, so that lower frequency band below 35 kHz is avoided in which most high-power switching devices are very active.

Table 1 Key parameters of the PHY specification

Issues	Value
Sample Frequency(MHz)	1.2
Space between subcarriers(kHz)	4.6875
Occupied Spectrum Band(kHz)	37.5 ~ 482.8125
Modulation scheme	ROBO/DBPSK/ DQPSK/D8PSK
Number of Preamble symbols	9.5
Number of FCH symbols	7
Length of FFT/IFFT points	$N_{FFT/IFFT} = 256$
Number of Available Subcarriers	$N = 96$
Number of Cyclic Prefix samples	$N_{CP} = 30$
Number of Overlapping samples	$N_{overlap} = 8$

2 Real-time DSM algorithm

2.1 Mathematical model of DSM

The bandwidth of each subcarrier in HNPLC system is narrow enough in which the colored noise can be regarded as AWGN. BER/SER expression of the AWGN channel, which has connected SNR with transmission rate, provides an efficient guide for resources allocation.

Symbol error rate of the M-ary DPSK system $P_{Mn,\mathrm{DPSK}}$ is formulated as

$$P_{M_n,DPSK} \approx 2Q\left(\sqrt{2p_n g_n \sin^2\left(\frac{\pi}{\sqrt{2}M_n}\right)}\right) \tag{1}$$

where p_n is the allocated power of subcarrier n. g_n is the SNR for unit power. M_n is the constellation size and can be used to obtain data rate r_n as $r_n = \log_2(M_n)$. The mark number of the subcarrier satisfies $n \in \{1, 2, 3, \cdots N\}$ and N is the pre-determined number of legal subcarriers. Q-function is defined as

$$Q(\nu) = \frac{1}{\sqrt{2\pi}}\int_{\nu}^{\infty} \exp\left(-\frac{x^2}{2}\right) dx \tag{2}$$

Eq. (1) can be restated as

$$p_n = \frac{\left[Q^{-1}\left(\frac{P_{M_n,DPSK}}{2}\right)\right]^2}{2g_n \sin^2\left(\frac{\pi}{\sqrt{2}M_n}\right)} \tag{3}$$

Let ρ_n be the state indicator function of subcarrier n, which satisfies

$$\rho_n = \begin{cases} 1, & \text{if subcarrier } n \text{ is on} \\ 0, & \text{if subcarrier } n \text{ is off} \end{cases} \tag{4}$$

Then the objective is to maximize the data rate

$$F = \max \sum_n \rho_n r_n \tag{5}$$

with the constraint of

$$\sum_n \rho_n p_n \leqslant W \tag{6}$$

where W is the authorized transmission power.

2.2 Design of real-time DSM

It is necessary for the real-time DSM to not only meet the real-time demand of low overhead cost and low complexity, but also do the best to approach the optimal bit-loading performance. Thus in the proposed algorithm, subcarriers are adaptively chosen in group and only one modulation scheme is employed within each transmission[27,28]. The proposed algorithm is also merged, transformed and simplified in the following description to facilitate the corresponding design of FPGA circuit.

Split the overall N subcarriers into I groups. Then there are $I' = N/I$ subcarriers in each group. Redefine $\rho_i (i \in \{1, 2, \cdots, I\})$ as the state indicator function of sub-group i to instruct the turning on ($\rho_i = 1$) or shutting down ($\rho_i = 0$). Then the real-time DSM is carried out as follows.

2.2.1 Step 1: To determine the value of Γ

Let M be the constellation size and assume that a bit error corresponds to a symbol error. Then the relation between $P_{M,\mathrm{DPSK}}$ and BER e is

$$P_{\mathrm{M,DPSK}} = \begin{cases} C_4^2 \times e = 6e, & \text{ROBO} \\ \dfrac{e}{\log_2^M}, & \text{others} \end{cases} \tag{7}$$

C_a^b presents the selection of b taken from a. Substituting Eq. (7) into Eq. (3), the allocated power of subcarrier n is obtained as follows:

$$p_n = \begin{cases} \dfrac{[Q^{-1}(3e)]^2}{2g_n \sin^2\left(\dfrac{\pi}{2\sqrt{2}}\right)}, & \text{ROBO} \\ \dfrac{\left[Q^{-1}\left(\dfrac{e}{2\log_2^M}\right)\right]^2}{2g_n \sin^2\left(\dfrac{\pi}{\sqrt{2}M}\right)}, & \text{others} \end{cases} \tag{8}$$

Define Γ as

$$\Gamma = \begin{cases} \dfrac{[Q^{-1}(3e)]^2}{2\sin^2\left(\dfrac{\pi}{2\sqrt{2}}\right)}, & \text{ROBO} \\ \dfrac{\left[Q^{-1}\left(\dfrac{e}{2\log_2^M}\right)\right]^2}{2\sin^2\left(\dfrac{\pi}{\sqrt{2}M}\right)}, & \text{others} \end{cases} \tag{9}$$

Then Eq. (8) is

$$p_n = \Gamma g_n^{-1} \tag{10}$$

As shown in Eq. (9), Γ is a function of modulation scheme and BER e. Since BER corresponds to the transmission quality, it is always pre-determined to fit various practical applications. In industry projects, BER is always selected as 10^{-3}, 10^{-4}, 10^{-5} or 10^{-6}. Hence Γ can be enumerated for different modulation schemes which can be easily achieved by a look up table (LUT) in the hardware implementation. Table 2 lists the values of Γ for the specific DPSK system.

Table 2 Values of Γ for the specific DPSK system

BER	Value of Γ			
	ROBO	DBPSK	DQPSK	D8PSK
10^{-3}	4.702	6.743	17.176	58.603
10^{-4}	7.334	9.427	24.877	86.968
10^{-5}	10.029	12.151	32.716	115.895
10^{-6}	12.760	14.902	40.640	145.164

2.2.2 Step 2: To determine group coefficient ρ_i

g_n^{-1} in Eq. (10) is the noise to signal ratio (NSR) which is the reciprocal of g_n. In order to avoid repeated division within the global scope, $1/g_n$ is estimated in SNR estimation module. Then NSR of each subgroup can be presented by S_i as

$$S_i = \sum_{n=i}^{i+I'-1} g_n^{-1}, \quad i \in \{1,2,3,\ldots,I\} \tag{11}$$

where I is the number of sub-groups. I' is the number of subcarriers in each sub-group.

Sort S_i in ascending order to get a new sequence $\tilde{S}_i^j$. The subscript i represents the original index in sequence S_i. Superscript j is the current index in the sorted sequence. The curve upon is used to distinguish the original and the sorted sequence.

Under the constraint of transmission power W, number l of selected sub-groups in each modulation scheme should satisfy:

$$\begin{cases} \Gamma \times \sum_{j=1}^{l} \tilde{S}^j \leqslant W \\ \Gamma \times (\tilde{S}^{l+1} + \sum_{j=1}^{l} \tilde{S}^j) > W \end{cases} \tag{12}$$

Corresponding to the selected sub-group $j(j \in \{1, 2, 3, \cdots, l\})$, the original index i ($l \leqslant I$, $i \in \{1, 2, 3, \cdots, I\}$) is got. Hereupon for the selected sub-group i, $\rho_i = 1$, otherwise $\rho_i = 0$.

For each modulation scheme, the number of selected sub-groups can be calculated by

$$l = \sum_i \rho_i \tag{13}$$

2.2.3 Step 3: To select modulation scheme

The number of selected sub-groups for different schemes are named as l_{ROBO}, l_{DBPSK}, l_{DQPSK} and l_{D8PSK}. They are achieved separately through previous steps. Then transmission rate of each scheme is expressed as Eq. (14), where ΔB is the frequency space of adjacent subcarriers.

$$\begin{cases} R_{\mathrm{ROBO}} = 0.25 l_{\mathrm{ROBO}} \times (I' \times \Delta B) \\ R_{\mathrm{DBPSK}} = l_{\mathrm{DBPSK}} \times (I' \times \Delta B) \\ R_{\mathrm{DQPSK}} = 2 l_{\mathrm{DQPSK}} \times (I' \times \Delta B) \\ R_{\mathrm{D8PSK}} = 3 l_{\mathrm{D8PSK}} \times (I' \times \Delta B) \end{cases} \tag{14}$$

Working out the maximum value of sequence $\{0.25 l_{\mathrm{ROBO}}, l_{\mathrm{DBPSK}}, 2 l_{\mathrm{DQPSK}}, 3 l_{\mathrm{D8PSK}}\}$, the best modulation scheme is selected as

$$\begin{aligned} &\arg\max\{R_{ROBO}, R_{DBPSK}, R_{DQPSK}, R_{D8PSK}\} \\ &\quad = \arg\max\{0.25 l_{ROBO}, l_{DBPSK}, 2 l_{DQPSK}, 3 l_{D8PSK}\} \end{aligned} \tag{15}$$

2.2.4 Step 4: To allocate residual power

Corresponding to the recommended modulation scheme and the allocated power p_n of each selected subcarrier, there is generally some power left which does not meet the equal sign in Eq. (6). In order to further improve system performance under constraint of transmission power W, the calculated power p_n could be multiplied by a power coefficient λ. Then the final allocated power of each selected subcarrier is

$$p'_n = \lambda p_n = \frac{W}{\Gamma \times \sum_i \rho_i S_i} \times (\Gamma g_n^{-1}) = W \frac{g_n^{-1}}{\sum_i \rho_i S_i} \tag{16}$$

3 Performance simulation of the real-time DSM

3.1 Performance improvement of the real-time DSM

The performance of the real-time DSM is firstly simulated via an AWGN multi-path channel to obtain a reference boundary. Actually in practical systems, it is reasonable to regard that the noise is AWGN in each subcarrier due to the clipping in the analog front end (AFE).

The simulated SNR is set upon −10dB in order to guarantee a reliable synchronization. BER of different modulation schemes are illustrated in Fig. 2. The adopted HNPLC channel in the simulation is a 14-path model obtained by LMMSE-based curve fitting of the measured channel[29].

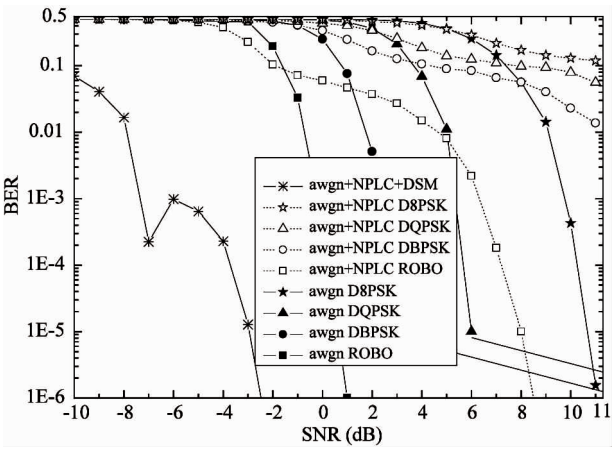

Fig. 2 Simulated BER of different modulation schemes

It is shown in Fig. 2 that multipath severely degrades BER. However, applying the real-time DSM, performance is significantly improved because of the adaptive shutdown for those deeply notched subgroups. As the subgroup is the basic unit to perform turning on or shutting off, it begets the BER jump due to the discontinuous selection of subcarriers.

3.2 Tradeoff of real-time DSM

Overhead and complexity of the proposed DSM and the optimal Hughes-Hartogs algorithm are compared in Table 3. It shows that both computational complexity and overhead cost are greatly reduced in the real-time DSM, which confirms the feasibility of being applied to the practical real-time systems.

Table 3 Comparison of overhead and complexity

	Overhead (bit)	Power calculation operations (times)	Search operations (times)
Hughes-H.	192	4×96	$96 \times M$
Proposed DSM	26	4×96	96

On the other hand, the performance of the proposed DSM shall inevitably decrease comparing with the optimal bit-loading algorithm. Fig. 3 shows the data rate comparison when transmission power changes. It shows that the rate gap between the real-time DSM and the optimal Hughes-Hartogs algorithm is tiny and the proposed DSM is suitable for industry applications[28].

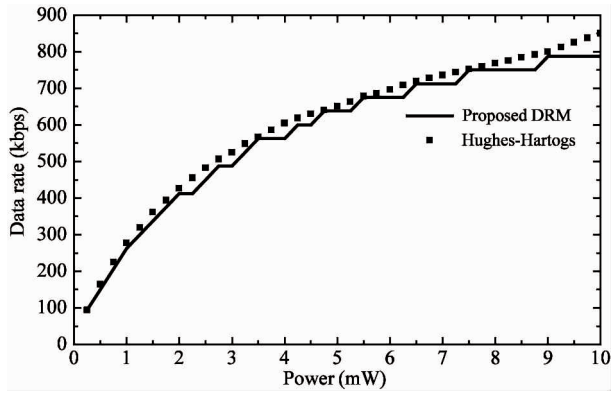

Fig. 3 Data rate comparison of the real-time DSM and the Hughes-Hartogs algorithm when transmission power changes

4 Hardware implementation of the real-time DSM

Detailed description of hardware implementation of the real-time DSM is presented in this section. The legal 96 subcarriers (see Table 1) are spited into 24 subgroups, while each subgroup contains four subcarriers.

4.1 Implementation diagram

Fig. 4 is the schematic implementation of the proposed DSM. For clarity, some control signals and aided data are omitted in this figure. Requested BER e oriented for different services and authorized transmission power W need to be set by the higher layer. The NSR valid signal initializes the DSM module and the p'_n valid signal indicates the successful output by the DSM module. The assisted valid signals are not illustrated in Fig. 4. However their timing sequence is shown in Fig. 5.

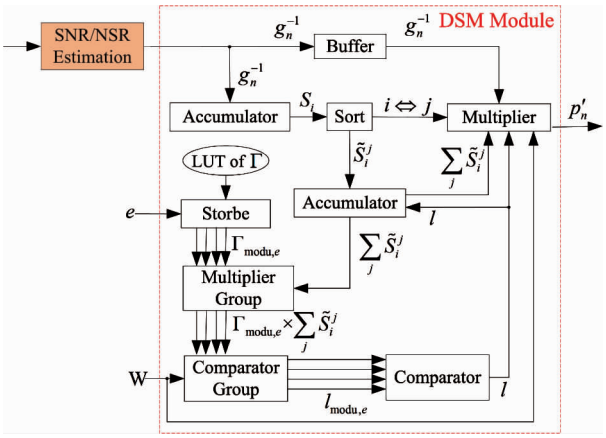

Fig. 4 Schematic implementation of the proposed DSM

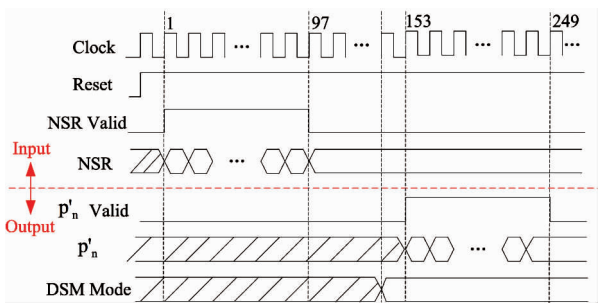

Fig. 5 Timing diagram of the proposed DSM

4.2 Resource management and timing sequence

Conversions of arithmetic operations can further reduce the resource cost. The numbers of various arithmetic operations without or with conversions are shown in Table 4, where $\sum l$ is the sum of l_{ROBO}, l_{DBPSK}, l_{DQPSK} and l_{D8PSK}. l_{selected} represents the number of selected subgroups under the selected modulation scheme ($l_{\mathrm{selected}} \in \{l_{\mathrm{ROBO}}, l_{\mathrm{DBPSK}}, l_{\mathrm{DQPSK}}, l_{\mathrm{D8PSK}}\}$). It shows that more than 171 multiplication operations are saved with conversions. And the division is harshly reduced without accuracy loss by adding only one LUT.

Table 4 The numbers of various arithmetic operations without or with conversions

	Addition	Multiplication	Division	LUT
Without conversions	$287 + \sum l$	196	97	0
With conversions	$290 + \sum l$	$l + 1$	1	1

Timing diagram of the proposed DSM under the framework of the specific HNPLC system is shown in Fig. 5. It costs 249 clock cycles and about 207 μs to output the decision, which is less than the time of an OFDM symbol. This means that the implementation of DSM circuit conforms to the real-time demand of HNPLC applications.

5 Network experiments

5.1 Hardware implementation of the HNPLC PHY system

Hardware implementation of the specific HNPLC PHY system with real-time DSM is illustrated in Fig. 6 with the development platform of Xilinx KC705[30].

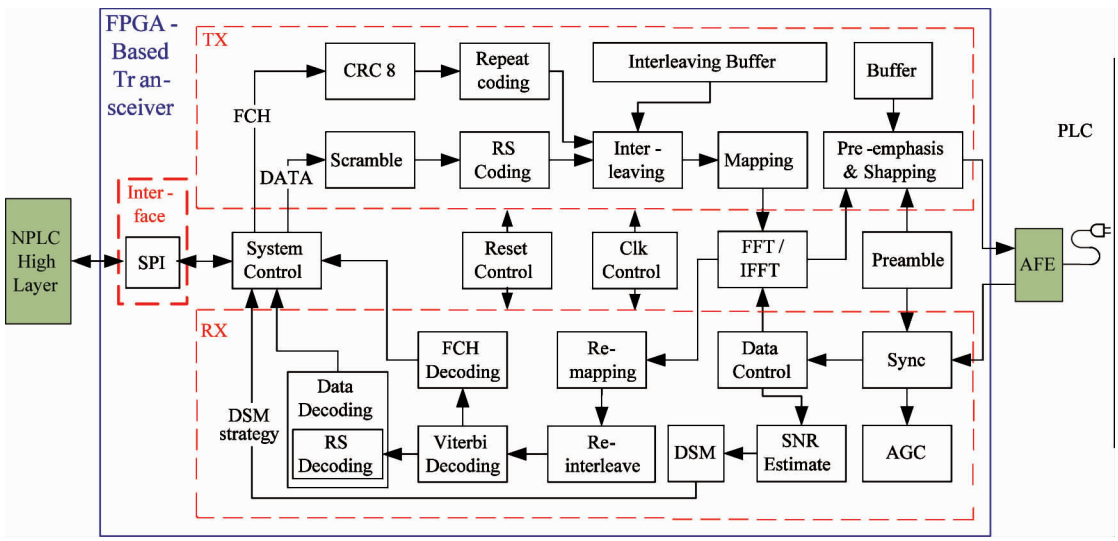

Fig. 6 Hardware implementation of the specific PHY system

As shown in Fig. 6, the transceiver's physical layer includes three main modules of interface circuit, transmitter (TX) and receiver (RX). Serial peripheral interface (SPI) is used to exchange data between

the physical layer and the higher layer. TX and RX work separately with a sharing FFT/IFFT module. Additionally, there are self-governed clock control module and reset control module to facilitate system debug. System control module acts as the coordinator.

Taking advantages of the integrated design tool of Vivado, the system resource consumption of the specific HNPLC PHY system is recorded in Table 5. This PHY implementation consumes less than two million logical gates and about 40% resource of XC7K325T-2FFG900C (FPGA on KC705).

Table 5 System resource consumption of the specific HNPLC PHY system

Item	Available	Usage	Occupancy Rate
FF	407600	14501	4%
LUT	203800	31272	15%
Memory LUT	64000	1258	2%
I/O	500	83	17%
BRAM	890	22	2%
DSP48	840	71	8%
BUFG	32	30	94%
PLL	10	1	10%

5.2 Experiment setup

The experimental test bed is shown in Fig. 7. The real-time DSM can be optionally adopted via control of personal computer (PC). DSM ploy is recorded and saved to evaluate the effectiveness. AFE acts as the suitable coupler which consists of the filter and amplifier circuit (FAC) and FMC150 (the ADC-DAC daughter card for KC705)[31]. The arrows in Fig. 7 stand for the data flow while squares present electrical appliances.

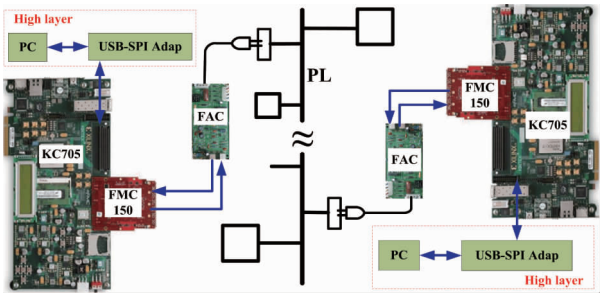

Fig. 7 The experimental test bed

5.3 Practical results of the real-time DSM

The transmission data from the reserved I/O pins of KC705 and PHY registers are recorded by a logic analyzer at the same time. The constellation of received data is shown in Fig. 8(a) without applying the real-time DSM. In comparison to it, the constellation enabling DSM is shown in Fig. 8(b). It is obvious that the constellation has been significantly improved by the real-time DSM. Fig. 9 shows the responding power allocation offered by the on-going DSM. Fig. 9(a) is the estimated SNR and Fig. 9(b) is the power allocation for the subcarriers. In this case, 11 sub-groups, 44 out of 96 subcarriers, are selected to load bits while other sub-groups are abandoned. The proposed modulation scheme by the real-time DSM is D8PSK. This power allocation also indicates the implied rule that the higher quality the channel is, the less power it needs for a specified transmission in which abandoned subcarriers are allocated no power.

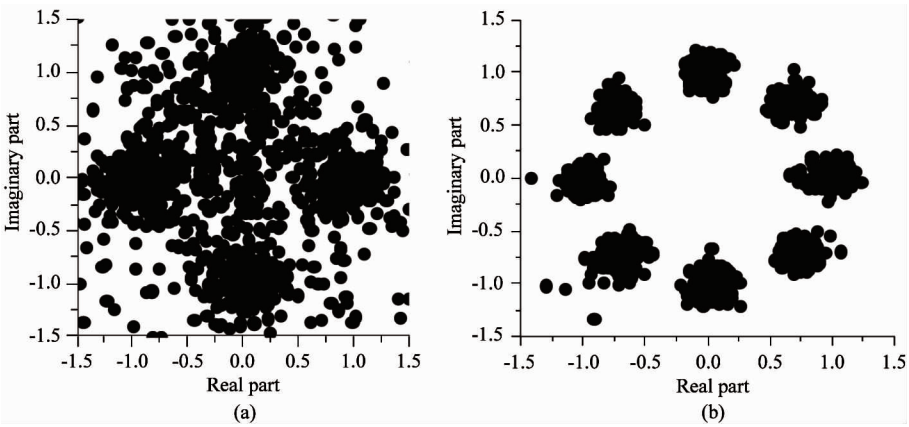

Fig. 8 Constellation of received data (a) without and (b) with the proposed DSM

5.4 System performance

Package error rate (PER) is counted to evaluate the system performance. Table 6 lists the PER of the ordinary DBPSK with equal power allocation and the PER of real-time DSM in the HNPLC system under different scenarios of the practical indoor power line environment. The results reveal that PER is reduced dramatically, e. g. in scenario 1 from 33.3% to 1.0%.

It is verified that the real-time DSM is available and system robustness is improved obviously by employing the proposed real-time DSM.

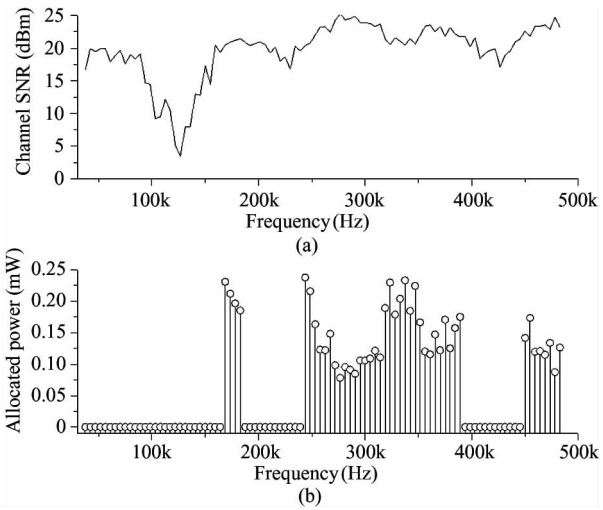

Fig. 9 (a) Estimated SNR (b) Subcarriers power allocation of the real-time DSM

Table 6 PER of ordinary DBPSK and the real-time DSM in the HNPLC system

	1	2
PER of ordinary DBPSK	33.3%	44.3%
PER of real-time DSM	1.0%	1.1%

6 Conclusions

OFDM-based HNPLC offers reliable, economical and efficient information transmissions for smart grid applications such as AMI, intelligent micro grids, charging and discharging management of EV and so on. In order to combat the time-varying frequency selective attenuated and colored noisy channel of practical HNPLC system, this study proposes a real-time DSM for the OFDM-based HNPLC system. The proposed real-time DSM employs the formulated expression of BER/SER for power allocation since the noise in each narrow subcarrier is approximately Gaussian. To realize the real-time requirement and obtain the low overhead cost and low computational complexity, the proposed DSM chooses subcarriers in group and adopts the same modulation scheme in each transmission. Some flexible and efficient conversions are also detailed and implemented in the design and hardware realization of the real-time DSM. Practical networked experiments are executed with KC705 in the real power line environment and corresponding results validate the performance enhancement of the proposed real-time DSM.

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Liu Wenjing, born in 1984. She is currently a PhD candidate in the Department of Electrical Engineering, Tsinghua University, China. She received her B. S degree in electronic information science and technology from Shandong Normal University (2007) and received her M. S degree in control theory and control engineering from Beijing Technology and Business University (2010). Her research interests include power line communication and smart grid technologies.