doi:10.3772/j.issn.1006-6748.2014.01.015

Design of 15 Gb/s inductorless limiting amplifier with RSSI and LOS indication in 65nm CMOS①

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Abstract

A limiting amplifier IC implemented in 65nm CMOS technology and intended for high-speed optical fiber communications is described in this paper. The inductorless limiting amplifier incorporates 5-stage 8 dB gain limiting cells with active feedback and negative Miller capacitance, a high speed output buffer with novel third order active feedback, and a high speed full-wave rectifier. The receiver signal strength indictor (RSSI) can detect input signal power with 33dB dynamic range, and the limiting amplifier features a programmable loss of signal (LOS) indication with external resistor. The sensitivity of the limiting amplifier is 5.5mV at BER = 10^{-12} and the layout area is only 0.53 × 0.72 mm^2 because of no passive inductor. The total gain is over 41dB, and bandwidth exceeds 12GHz with 56mW power dissipation.

Key words: limiting amplifier, receiver signal strength indictor (RSSI), loss of signal (LOS), full-wave rectifier, third order active feedback

0 Introduction

The exponential growth of data traffic has created high demand for electronic components working at 10Gb/s for optical fiber systems. Limiting amplifiers are the critical building block of optical receivers. In the past, most ICs at data rates of Gb/s are manufactured in GaAs or SiGe technologies with higher cost and higher power dissipation[1-4]. The CMOS technology, on the contrary, has the merits of lower cost, lower power dissipation and highest integration capacity. However, CMOS devices present difficult challenges in the design of limiting amplifiers with RSSI and LOS indication working over 10 Gb/s bit rate. Recently, several limiting amplifiers realized in the CMOS technology of 10 Gb/s have been reported[5-7], but none of them can perform receiver signal strength indictor (RSSI) or loss of signal (LOS) indication. For industrial and commercial applications, these two functions must be considered for reliability in the IC design of limiting amplifiers.

The output voltage of RSSI is in logarithm with the amplitude of input pseudo random bit sequence (PRBS). Due to the squeezing properties of the logarithmic function, the detecting range of RSSI can be extended, which is suitable for low supply voltage in 65nm CMOS technology. The LOS indicator can monitor insufficient optical power and detect system fault which will result in excessive bit errors. Different systems have different demands for bit errors, thus LOS must have programmable threshold voltage to detect whether the amplitude of input signal meets the application requirements.

1 Limiting amplifier architecture

The limiting amplifier of this paper has fully differential architecture as shown in Fig. 1, which consists of an input buffer with dc offset subtractor (DOS),

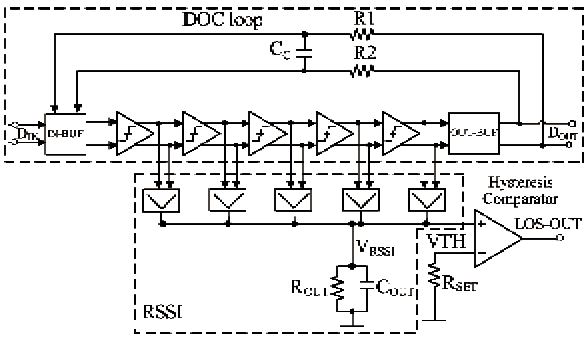

Fig. 1 Limiting amplifier architecture

① Supported by the National High Technology Research and Development Programme of China (No. 2011AA010301) and the National Natural Science Foundation of China (No. 60976029).

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Received on Mar. 1, 2012

five-stage limiting cells, an output buffer, a dc offset cancellation (DOC) feedback loop, a RSSI circuit, and a LOS indication circuit.

1.1 RSSI

A logarithmic amplifier is widely used in RSSI, since a wide dynamic variation of signal power can be represented within limited voltage range. But in CMOS technology, a true logarithmic amplifier couldn't be realized. As shown in Fig. 1, successive detection is based on piecewise linear approximation. Each part is realized by rectifying each limiting cell's output. The precision of RSSI is mainly dominated by the number of limiting cells. The maximum error compared with an ideal logarithmic curve can be derived as Ref. [8]:

$$\mathrm{Error}_{\max}(\mathrm{dB}) = \frac{10[(-1+\sqrt{A_S}+A_S)\log A_S-(A_S-1)\log(A_S^{\frac{3A_S-1}{2A_S-1}})]}{A_S-1} \quad (1)$$

where A_S in Eq. (1) is the gain of each limiting cell. When using 5-stage limiting cells in the architecture and the gain of each cell is 8dB, the relative error in RSSI is less than 0.5dB, which meets most of application occasions.

1.2 LOS indication

LOS indication circuit is an important module in the limiting amplifier, which outputs a binary signal indicating whether the amplitude of input signal is lower than the threshold voltage for given bit errors. The output voltage of RSSI is logarithmic with the input voltage, which can be expressed as

$$V_{\mathrm{RSSI}} \approx V_0 + k \cdot \log V_{\mathrm{in}} \quad (2)$$

where V_{in} is the input voltage amplitude, V_0 and k are constant for a given design. The LOS has two kinds of input voltages: assert voltage (V_{assert}) and de-assert voltage ($V_{\mathrm{de\text{-}assert}}$), and optical hysteresis (H) is defined as

$$H = 20 \times \log\left(\frac{V_{\mathrm{de\text{-}assert}}}{V_{\mathrm{assert}}}\right) \quad (3)$$

The optical hysteresis is typically set to 3dB. As shown in Fig. 1, VTH pin sets the assert threshold voltage V_{TH}, and the hysteresis comparator compares V_{RSSI} and V_{TH}. When V_{RSSI} falls below V_{TH}, the hysteresis comparator outputs high voltage indicating LOS occurred. As the input voltage rises, V_{RSSI} rises logarithmically. When V_{in} rises up to $V_{\mathrm{de\text{-}assert}}$ and at the same time V_{RSSI} is a comparator's hysteresis width over V_{TH}, the comparator outputs low voltage level, indicating LOS is de-asserted.

2 Circuit design

2.1 8-dB gain limiting cell

The limiting cell is shown in Fig. 2, which is based on the second-order active feedback circuit, and M3-4, R3-4, M5-6, R1-2 constitute the active feedback loop. Compared to traditional Cherry-Hooper amplifier[9], active feedback does not resistively load the trans-impedance stage of the limiting cell. And thus active feedback has higher gain if the feedback factor is the same, which corresponds to higher gain-bandwidth product.

The total gain of the limiting amplifier is obtained by cascading several limiting cells; hence, the gate capacitance of next stage is directly added to the output of the previous limiting cell. M7-8 and M9-10 constitute negative miller capacitance, which is employed to cancel out part of the gate capacitance, and hence boosts the total bandwidth. The negative miller capacitance is realized by using MOS varactors instead of MIM capacitors because MIM capacitors occupy large chip area. However, the capacitance is variable as the voltage across the varactor changes. To guarantee the negative miller capacitance constant even though the voltage across the capacitors changes, two MOS varactors are paralleled with the opposite connection as shown in Fig. 2.

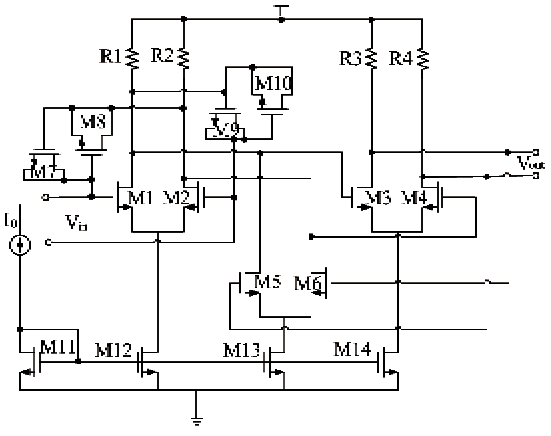

Fig. 2 Limiting cell with second-order active feedback circuit

2.2 Output buffer

The output buffer driving off-chip loads typically present a bandwidth bottleneck resulting from the large input transistors that are necessary for high current drive capability. To deliver differential voltage swing of 0.6V to equivalent 25Ω output resistance, the buffer must steer 12mA current.

This work employs a novel three-order active feedback circuit in the output buffer. As shown in Fig. 3,

M1-2, R1-2 compose the first differential amplifiers (DA1), M3-4, R3-4 constitute DA2, M5-6, R5-6 form DA3, and M7-8, R1-2 form DA4. DA1 and DA2 are two-stage differential pairs used to minimize the capacitance load to the previous limiting cell.

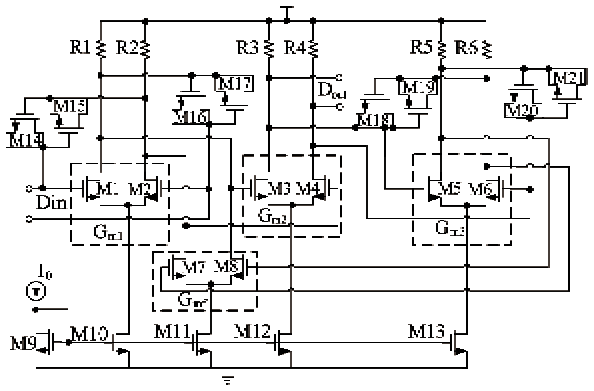

Fig. 3 Output buffer with the third-order active feedback circuit

Hence the bandwidth bottleneck moves to the output of DA1 where the large capacitance from DA2 directly loads to it. Minimizing the resistance of R1 and R2 or using inductor peaking is commonly used to broaden the bandwidth, but the value of R1 and R2 must be low enough to increase the speed of the buffer which leads to output swing of DA1 too small to switch the DA2 effectively. Using inductor peaking is the other choice but it will increase chip area significantly. This paper presents a novel third-order active feedback technology to increase the speed of the output buffer. DA2, DA3 and DA4 consist of feedback loop, compared to traditional third-order active feedback, the output is from DA2 not from DA3. The width of M3 and M4 can be increased but the speed of the overall buffer is remained almost the same. As the width of M3 and M4 increase, the overdrive voltage of DA2 decreases, thus DA2 can be switched more effectively. The output of DA3 is connected to the low pass filter of the DOC loop, therefore DA3 composes part of DOC loop. The other role of DA3 is in DOC which will be analyzed in the next section. The MOS varactors M14-17 are used as negative miller capacitance to cancel part of the output capacitance of the last limiting cell, and M18-21 are used to cancel a portion of output capacitance of DA2.

2.3 Input buffer and DOC loop

The input buffer and dc offset subtractor are shown in Fig. 4, where M1-2 constitute the trans-conductance stage of input buffer and M3-4 constitute the trans-conductance stage of the dc offset subtractor. M5, M7 and R3 generate the bias of input common-mode level which is a replica of the input buffer, but the size of the component is scaled. R4 and R5 are 50Ω resistors which consist of input matching network.

The DOC feedback loop is made up of limiting amplifier with the output buffer, low pass filter (LPF), and DOS. Supposing that the gain of DOS is A_1, the gain of limiting amplifier is A_2, and the gain of DA3 is A_3, the closed loop dc gain (A_{dc}) is

$$A_{dc} = \frac{A_2}{1 - A_1 \cdot A_2 \cdot A_3} \approx \frac{1}{A_1 \cdot A_3} \tag{4}$$

From Eq. (4), the dc gain of A_{dc} is A_3 times less than that without using DA3, thus the output offset voltage is minimized, and this is the function of DA3 in the DOC.

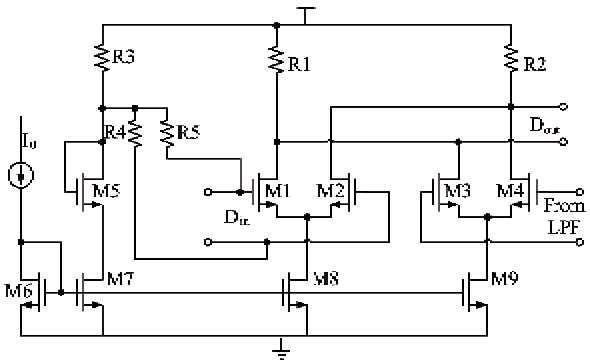

Fig. 4 Input buffer and dc offset subtractor

2.4 Full-wave rectifier

The rectifier and V/I converter constitute the RSSI. The high speed rectifier is shown in Fig. 5. M1-2 and M6 compose the core of rectifier, of which the output voltage is a function of the input signal's power. The input voltage can be written as

$$V_{in1} = V_{CM} + V_{in}/2; \quad V_{in2} = V_{CM} - V_{in}/2 \tag{5}$$

where V_{CM} is the input common mode voltage, V_{in} and V_0 are the input differential voltage and output voltage respectively. According to the case that drain current of M1 and M2 equals to I_b:

$$\frac{1}{2}K_n\frac{W}{L}(V_{CM} + V_{in}/2 - V_0 - V_{th})^2 + \frac{1}{2}K_n\frac{W}{L}(V_{CM} - V_{in}/2 - V_0 - V_{th})^2 = I_b \tag{6}$$

where K_n is a constant value for a given channel length, W and L are the width and length of M1 and M2, V_{th} is the threshold voltage of M1 and M2, I_b is the bias current of M1 and M2. From Eq. (6), V_0 can be obtained as

$$V_0 = V_{CM} - V_{th} - \sqrt{\frac{I_b}{K_n\frac{W}{L}} - \frac{V_{in}^2}{4}} \tag{7}$$

Eq. (7) shows that M1-2 and M6 can rectify the input differential voltage. M3-4 and M7 are the replica of M1-2 and M6 to produce the input common mode voltage for the V/I converter, and the components' size of which is scaled. Mp1 and Mp2 are the pre-filter capacitors realized in PMOS MOSFETs.

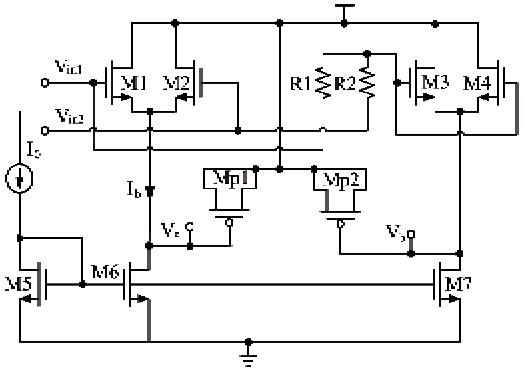

Fig. 5 High speed rectifier

2.5 Hysteresis comparator

The hysteresis comparator is based on positive feedback to produce hysteresis. As shown in Fig. 6, where Mp1-4 compose positive feedback loop, and Mp1, Mp4 have the same size with width to length ratio set to β_1; the width to length ratio of Mp2 and Mp3 is β_2. When $\beta_2/\beta_1 > 1$, the comparator produces hysteresis, but when $\beta_2/\beta_1 < 1$, the hysteresis disappears. M5-6 and Mp5-6 build up class AB output stage to provide reasonable output voltage swing and output resistance[10].

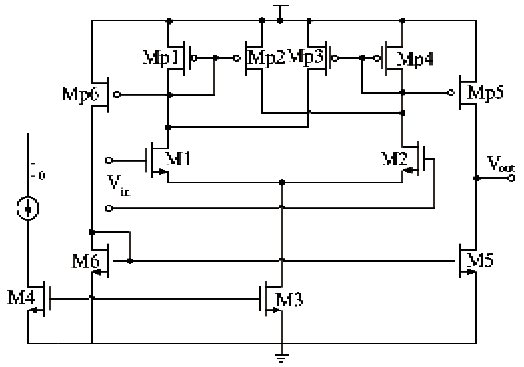

Fig. 6 The hysteresis comparator

3 Layout and post simulation results

The limiting amplifier with RSSI and LOS indication is designed in TSMC 65nm 1P9M CMOS technology. The layout is shown in Fig. 7 with an area only of $0.53 \times 0.72\text{mm}^2$ (including bonding pad) because of no inductor. The N + guard ring and P + guard ring isolation structure is used in the output buffer to suppress the noise coupled to the limiting cells by substrate.

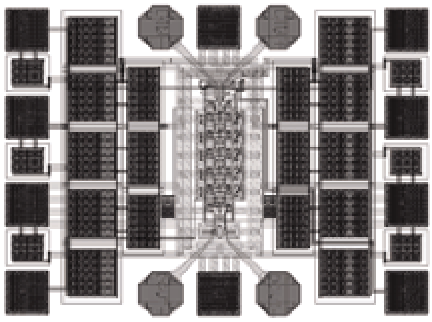

Fig. 7 Layout of limiting amplifier

A spectra RF circuit simulator is used to analyse the frequency response and transient characteristic of the limiting amplifier. Fig. 8 illustrates the frequency response of the limiting amplifier. The total gain is 41.69dB, and the low and high cut-off frequency is 41kHz and 12.4GHz respectively. Fig. 9 depicts the 15Gb/s output eye diagram of the limiting amplifier corresponding to 5.5mV peak to peak input. The output voltage of RSSI versus the amplitude of input PRBS is shown in Fig. 10. The linear region of the curve starts from 5mV input voltage and ends at 237mV, corresponding to 33.5dB detection dynamic range. This limiting amplifier with LOS indication chip has been taped out in 65nm CMOS technology and the corresponding experimental results will be given subsequently.

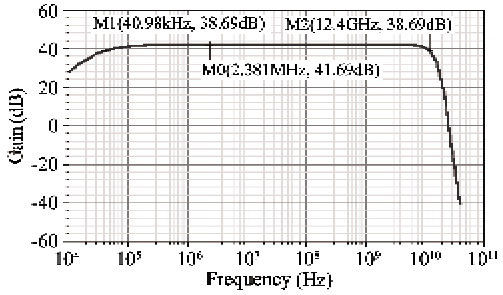

Fig. 8 Frequency response of limiting amplifier

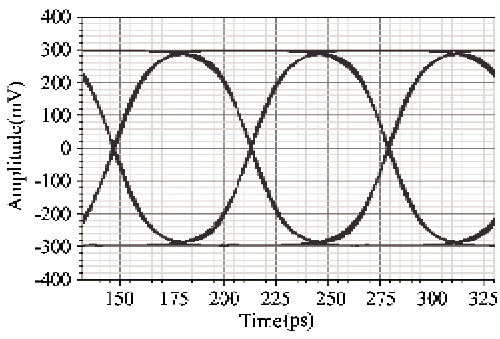

Fig. 9 15 Gb/s eye diagram for input level of 5.5mV

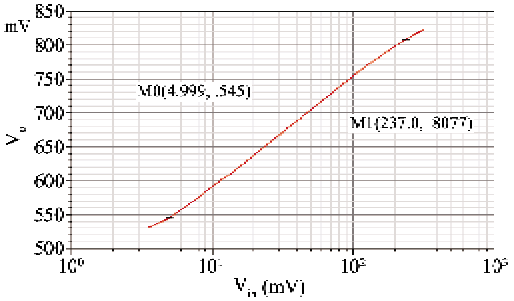

Fig. 10 The output voltage of RSSI versus input voltage

4 Conclusions

A limiting amplifier with RSSI and LOS indication for 15-Gb/s applications in 65nm CMOS technology is presented in this paper. The second-order active feedback and negative miller capacitance is used to extend the bandwidth of the limiting cells, and the varactors are used as negative miller capacitance to minimize the area of limiting cells. The output buffer is realized using a novel third-order feedback and the negative miller capacitance technology. The high speed full-wave rectifiers and V/I converters build up the RSSI circuit. The RSSI circuit and hysteresis comparator then compose the LOS indication circuit. The simulated result reveals that the limiting amplifier has the characteristic of low power, high speed and small occupied area, and the RSSI has a large detection range and good linearity.

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